

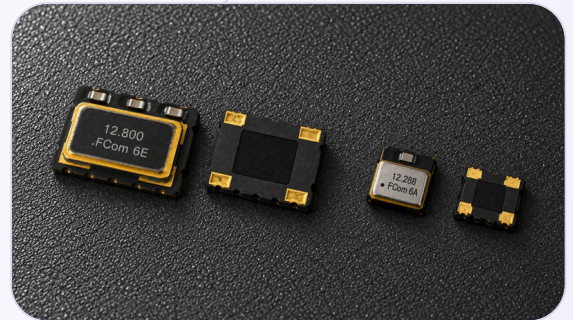
VOLTAGE CONTROLLED CRYSTAL OSCILLATORS

VCXO

Product Selection Guide

CMOS, LVPECL
& LVDS Outputs

2.5 V / 2.8 V
3.3 V Supply



Standard VCXO

Low Jitter VCXO

Differential VCXO

Up to 1500 MHz

One function. A choice of output and jitter class.

Compare the full VCXO range in a consistent, series-by-series list. Review package, frequency range, supply voltage, stability, temperature, output, pullability and phase noise before selecting a configuration.

08

Individual series
in one guide

03

Product groups
for comparison

1.5 GHz

Highest available
output frequency

+105 °C

Maximum operating
temperature

2 SERIES

Standard VCXO

FVC-3X and FVC-5X CMOS VCXO in 3225 and 5032 six-pad SMD packages, from 1.5 MHz to 170 MHz.

[Full selection list · Page 02](#)

3 SERIES

Low Jitter VCXO

FVC-3P-LJ, FVC-5P-LJ and FVC-7P-LJ CMOS VCXO with phase noise to -125 dBc/Hz at 10 kHz.

[Low jitter selection · Page 02](#)

3 SERIES

Differential VCXO

FVC-3L-PG, FVC-5L-PG and FVC-7L-PG with LVPECL or LVDS output up to 1500 MHz.

[Differential selection · Page 03](#)

Compare the series. Confirm the configuration.

Click a series name or View PDF to open its datasheet. Confirm the latest controlled specifications before placing an order.

01

Standard & Low Jitter VCXO

CMOS voltage controlled crystal oscillators in 3225, 5032 and 7050 six-pad SMD packages.
Each series is listed separately for direct comparison.

Output: CMOS · Supply: 2.5 V / 2.8 V / 3.3 V

5 SERIES · SURFACE MOUNT

Photo	Series	Package	Frequency range MHz	Supply voltage V	Stability ±ppm	Widest temp. °C	Output	Pullability ±ppm	Phase noise dBc/Hz	Datasheet PDF
Standard VCXO · CMOS output										2 SERIES
	FVC-3X	3225 6-SMD	2 - 66	2.8 / 3.3	±25 to ±50	-40 to +105	CMOS	±50 to ±150	— -107 -111 -114	View PDF ↗
	FVC-5X	5032 6-SMD	1.5 - 170	3.3	±25 to ±50	-40 to +105	CMOS	±50 (APR)	— -100 -133 -140	View PDF ↗
Low jitter VCXO · CMOS output										3 SERIES
	FVC-3P-LJ	3225 6-SMD	10 - 250	2.5 / 3.3	±25 to ±50	-40 to +105	CMOS	±50 to ±150	— -107 -111 -114	View PDF ↗
	FVC-5P-LJ	5032 6-SMD	10 - 250	2.5 / 3.3	±25 to ±50	-40 to +105	CMOS	±50 (APR)	— -75 -105 -125	View PDF ↗
	FVC-7P-LJ	7050 6-SMD	10 - 250	2.5 / 3.3	±25 to ±50	-40 to +105	CMOS	±50 (APR)	— -75 -105 -125	View PDF ↗

Phase noise column lists typical values at 100 Hz / 1 kHz / 10 kHz / 100 kHz offsets from the carrier. "—" indicates the value is not specified for that series. Product images are for identification. Refer to the series datasheet for exact dimensions, pad assignments and test conditions.

Read the parameters together

1. Stability options describe the frequency tolerance against a stated reference condition. They are not a full temperature stability specification and are not necessarily available in every combination with supply voltage, temperature range and pullability.

2. Pullability is quoted as APR (absolute pull range) unless otherwise noted. Confirm the applicable APR, control voltage range, linearity and polarity in the selected series datasheet.

3. Phase noise figures are typical values at the stated offset. Confirm the measurement bandwidth reference, output load and supply voltage before comparing series across different product groups.

02

Differential VCXO

LVPECL and LVDS voltage controlled crystal oscillators up to 1500 MHz in 3225, 5032 and 7050 six-pad SMD packages.

Output: LVPECL / LVDS · Supply: 2.5 V / 3.3 V

3 SERIES · SURFACE MOUNT

Photo	Series	Package	Frequency range MHz	Supply voltage V	Stability $\pm$ ppm	Widest temp. °C	Output	Pullability $\pm$ ppm	Phase noise dBc/Hz	Datasheet PDF
Differential VCXO · LVPECL / LVDS output										3 SERIES
	FVC-3L-PG	3225 6-SMD	10 - 1500	2.5 / 3.3	$\pm$ 25 to $\pm$ 50	-40 to +105	LVPECL LVDS	$\pm$ 50 to $\pm$ 150	— -107 -111 -114	View PDF ↗
	FVC-5L-PG	5032 6-SMD	10 - 1500	2.5 / 3.3	$\pm$ 25 to $\pm$ 50	-40 to +105	LVPECL LVDS	$\pm$ 50 (APR)	— -70 -95 -105	View PDF ↗
	FVC-7L-PG	7050 6-SMD	10 - 1500	2.5 / 3.3	$\pm$ 25 to $\pm$ 50	-40 to +105	LVPECL LVDS	$\pm$ 50 (APR)	— -70 -95 -105	View PDF ↗

LVPECL and LVDS outputs require the corresponding termination network. Phase noise column lists typical values at 100 Hz / 1 kHz / 10 kHz / 100 kHz offsets from the carrier. Images are for identification and are not to scale.

General clocking

FVC-3X · FVC-5X

2 - 170 MHz CMOS output in 3225 and 5032 packages, supply from 2.8 V.

Low phase noise

FVC-3P-LJ · FVC-5P-LJ · FVC-7P-LJ

10 - 250 MHz CMOS output with lower jitter for timing-sensitive designs.

High speed serial

FVC-3L-PG · FVC-5L-PG · FVC-7L-PG

10 - 1500 MHz LVPECL or LVDS output for SerDes and optical modules.

Before selecting an ordering code

1. Confirm the supply voltage, output type and load condition. LVPECL and LVDS outputs are not interchangeable with CMOS and require the corresponding termination.

2. Confirm stability, operating temperature range, APR and phase noise targets together. A single number taken in isolation does not describe the delivered performance.

3. Confirm the phase noise offset and measurement bandwidth reference in the series datasheet, and verify the required pullability against the oscillator IC control voltage range.

Need help matching a VCXO?

Share your preferred series, output type, supply voltage, pullability and oscillator IC with FCom for specification review.

Technical support ↗

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