

WIRELESS INFRASTRUCTURE

Wireless RAN & Base Stations

Timing, synchronization and RF solutions for 4G / 5G radio access infrastructure.

Frequency Stability + Synchronization + Low Phase Noise + Low Jitter + RF Filtering

Macro Base Stations

RU / RRH / AAU

DU / CU

Small Cells

Private 5G

Repeaters

Application Scope

Wireless access infrastructure requiring coordinated frequency and phase synchronization, stable RF reference clocks, low-jitter digital interfaces and application-specific RF filtering.

Relevant FCom Device Families

Primary: OCXO · TCXO / VCTCXO · VCXO · Standard / Low-jitter Differential XO · Quartz Crystal · SAW Filter

Architecture-dependent: MCF Crystal Filter

Timing

Frequency / phase synchronization, IEEE 1588 PTP, SyncE and holdover.

RF

RF reference generation, synthesizer and transceiver clocking.

Digital

FPGA, processor, SerDes, eCPRI and ADC / DAC reference clocking.

Filtering

RF front-end filtering and selected narrowband IF filtering.

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Application Scope & Engineering Domains

Identify the RAN subsystem first, then separate timing, RF, digital and filtering requirements.

Wireless RAN & Base Stations covers wireless access infrastructure requiring coordinated frequency and phase synchronization, stable RF reference clocks, network timing, low-jitter digital interfaces and application-specific RF filtering.

Typical Equipment

Radio Infrastructure

4G / 5G Macro Base Stations
Radio Units (RU)
Remote Radio Heads (RRH)
Active Antenna Units (AAU)

Distributed RAN

Distributed Units (DU)
Centralized Units (CU)
Wireless Infrastructure Gateways
Open Fronthaul / eCPRI

Coverage & Private Networks

Small Cells
Private 5G Infrastructure
Repeaters
Dedicated coverage nodes

Four Engineering Domains

Synchronization & Timing

Frequency synchronization ·
Phase synchronization ·
IEEE 1588 PTP · SyncE ·
Holdover timing

RF Reference Clocking

RF reference generation ·
RF synthesizer reference ·
RF transceiver clocking

Digital & Converter Clocking

FPGA / processor · ADC /
DAC · JESD · SerDes · High-
speed interface references

RF / IF Filtering

RF front-end filtering ·
Repeater / small-cell paths ·
Narrowband IF in selected
architectures

Main Technical Requirements

Synchronization

High frequency stability ·
Holdover performance ·
Temperature stability ·
Long-term aging control

RF Clocking

Low phase noise ·
Frequency stability ·
Temperature behavior ·
Spur control where
specified

High-Speed Digital

Low RMS jitter · Output-
interface compatibility ·
Signal integrity ·
Operating temperature

RF Filtering

RF selectivity · Insertion
loss · Ripple / rejection ·
Temperature behavior

Application note: FCom OCXO / TCXO / VCXO and XO families support precision timing, synchronization, RF references and system clocking. Quartz crystals are commonly used for local MCU, FPGA, SoC and management clocks when the receiving device includes a suitable oscillator circuit. SAW filters support selected RF signal paths, while MCF crystal filters apply primarily to narrowband IF or specialized radio architectures.

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Select by System Node First

Begin with the target clock or filter node, then determine the required frequency, performance class and device family.

Final requirements depend on the selected chipset, clock tree and RF architecture.

Representative FCom series are shown where they help connect the architecture to practical device selection; the final configuration remains application-specific.

System Node	Typical Function	Representative Frequency	Typical Device	Selection Focus
Timing / Holdover Module	Network synchronization and local continuity	10 / 20 / 30.72 / 38.88 MHz	OCXO / high-stability TCXO	Stability, aging, holdover, temperature, phase noise
Timing DPLL	PTP / SyncE local reference	20 / 25 / 30.72 / 38.88 MHz	TCXO / OCXO / VCXO	Stability, pullability, aging, DPLL input mode
RF PLL / Synthesizer	RF / LO reference generation	30.72 / 38.4 / 122.88 MHz	TCXO / VCXO	Phase noise, spurs, stability, tuning range
RF Transceiver / Converter	Radio and ADC / DAC reference clocking	38.4 / 122.88 MHz+	TCXO / VCXO / differential reference	Phase noise, jitter, output format, platform compatibility
FPGA / SerDes / eCPRI	High-speed processing and fronthaul	100 / 125 / 156.25 MHz+	Low-jitter differential XO	RMS jitter, LVDS/LVPECL/HCSL, signal integrity
MCU / SoC / Management	Local system clock	25 / 50 / 100 MHz	Quartz Crystal / CMOS XO	CL / ESR or supply/output, startup, package
RF Front End	Band selection / interference rejection	Band dependent	SAW Filter	Center frequency, bandwidth, insertion loss, rejection mask
Narrowband IF	High-Q IF / channel selectivity	Architecture dependent	MCF Crystal Filter	3 dB BW, stopband, ripple, insertion loss, impedance

Timing-Domain Selection

Where low-noise holdover is the priority, **FOC-5S-LN** is a representative FCom option. Compact or extended-temperature alternatives can be considered where size, power or environmental limits take priority.

RF-Clock Selection

Use VCXO / VCTCXO families where tuning or PLL control is required. **FVC-3P-LJ** is a representative 10–250 MHz CMOS VCXO option for reference nodes such as 122.88 MHz; confirm pull range, output format and phase-noise requirements for the target PLL.

Digital-Clock Selection

For 125 / 156.25 MHz differential REFCLK, **FCO-3L-UJ** is a representative 3225 option covering 100–220 MHz with LVPECL / LVDS / HCSL outputs and 50 fs listed RMS jitter.

Recommended selection sequence: System node → clock / filter role → external vs derived → frequency / band → performance → FCom series → final electrical configuration.

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Frequency & Component Placement Matrix

Evaluate representative frequencies together with system position, clock role and external / derived status before selecting a product family.

System Position	Typical Frequency	Primary Function	Reference / Applicability	Preferred Device
GNSS / Timing Module	10 MHz	Precision master / holdover reference	Common External Reference	OCXO
Timing DPLL	20 / 25 / 30.72 / 38.88 MHz	SyncE / PTP local reference	Common External Reference	TCXO / OCXO / VCXO
RF PLL / Synthesizer	30.72 / 38.4 / 122.88 MHz	RF / LO reference	Common External Reference	TCXO / VCXO
RF Transceiver	38.4 / 122.88 MHz	Radio-device reference	Platform-Dependent	TCXO / VCXO
JESD / Converter PLL	122.88 / 156.25 / 245.76 MHz	ADC / DAC reference clocking	Platform-Dependent	VCXO / differential XO
FPGA / DFE	100 / 125 / 156.25 MHz	Digital processing reference	Common External Reference	Low-jitter XO
eCPRI / Ethernet / SerDes	125 / 156.25 MHz	Transport / fronthaul REFCLK	Common External Reference	Differential XO
MCU / SoC / Management	25 / 50 / 100 MHz	Local system clock	Common External Reference	Crystal / CMOS XO
Radio Sampling / DFE Domains	61.44 / 184.32 / 245.76 / 307.2 / 491.52 MHz	Sampling / processing domains	Often Internally Derived	Do not assign an XO automatically
RF Front End	Band dependent	RF band selection / rejection	Application-Specific	SAW Filter
Narrowband IF	Architecture dependent	High-Q IF selectivity	Architecture-Dependent	MCF Crystal Filter

External Reference

Choose an FCom device only after confirming the documented external clock pin, output format and performance budget.

Derived Clock

PLL / DPLL / FPGA / transceiver domains can be much higher than the board-level reference and do not automatically need a separate oscillator.

Filter Path

For SAW / MCF selection, frequency alone is insufficient. Bandwidth, insertion loss, rejection mask, impedance and operating temperature must also be defined.

Selection note: this matrix focuses on clock placement and architecture. Representative FCom product families are introduced in the following platform and reference-design sections and summarized on Page 8.

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Representative RAN Platform & Clock Architecture Examples

The examples below illustrate documented clock-domain implementations in widely used RAN-oriented reference platforms. FCom products are shown by device function and capability range and should not be interpreted as validated drop-in replacements.

MICROCHIP

5G DU / CU Timing Architecture 1

Reference platform: MD-990-0011-B timing module with ZL80132B SyncE synchronizer and OX-221 OCXO.

Architecture insight: GNSS / SyncE / PTP inputs feed a dedicated synchronization and holdover domain; the local high-stability oscillator supports continuity during reference loss.

GNSS / PTP / SyncE → DPLL / Synchronizer → OCXO / ePPS

Representative FCom option: **FOC-5S-LN** — 10–40 MHz SMD OCXO with ± 5 ppb stability class, suitable for precision timing and holdover applications where low phase noise is required.

ANALOG DEVICES

ADRV904x Radio Clock Tree 2

Reference platform: ADRV904x EVB using AD9528 to create DEVCLK and SYSREF; the EVB includes a 122.88 MHz VCXO.

Architecture insight: a local VCXO and jitter cleaner form a clock-tree reference domain; the reference is distinct from RF carrier and internal converter clocks.

122.88 MHz VCXO → AD9528 → DEVCLK / SYSREF

Representative FCom option: **FVC-3P-LJ** — 10–250 MHz CMOS VCXO with ± 50 to ± 150 ppm pull range, suitable for tunable reference nodes such as 122.88 MHz when supported by the target PLL architecture.

TEXAS INSTRUMENTS

AFE79xx Base-Station RF Platform 3

Reference platform: AFE79xx EVM with LMK04828. TI documents an optional 10 MHz lab reference used to lock the onboard VCXO for synchronization and coherency.

Architecture insight: the upstream synchronization reference is separate from the high-rate RF-sampling ADC / DAC clock domains.

10 MHz External Sync → LMK04828 / VCXO → AFE79xx Clocking

FCom selection guidance: choose the precision OCXO or high-stability TCXO class according to the synchronization accuracy, holdover, temperature, aging and phase-noise requirements of the timing architecture.

ALTERA

O-RAN / eCPRI Fronthaul 4

Reference platform: O-RAN FPGA design examples use 156.25 MHz as an Ethernet hard-IP REFCLK on representative Agilex / Stratix implementations.

Architecture insight: eCPRI, PTP and TOD processing clocks are generated by internal IOPLL domains and must not automatically be interpreted as external oscillator requirements.

156.25 MHz REFCLK → Ethernet / SerDes → eCPRI / PTP IOPLL

Representative FCom option: **FCO-3L-UJ** — 100–220 MHz differential XO with LVPECL / LVDS / HCSL outputs, -40 to $+125^\circ\text{C}$ operating range and 50 fs listed RMS jitter.

Platform interpretation: these examples illustrate system-level clock roles and reference-clock placement. FCom products shown are representative capability matches only; final selection must be verified against the target IC documentation, electrical interface and complete system requirements.

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Macro / Distributed RAN Timing Architecture

Representative placement of FCom timing, processing and fronthaul reference families from upstream synchronization to the RU.

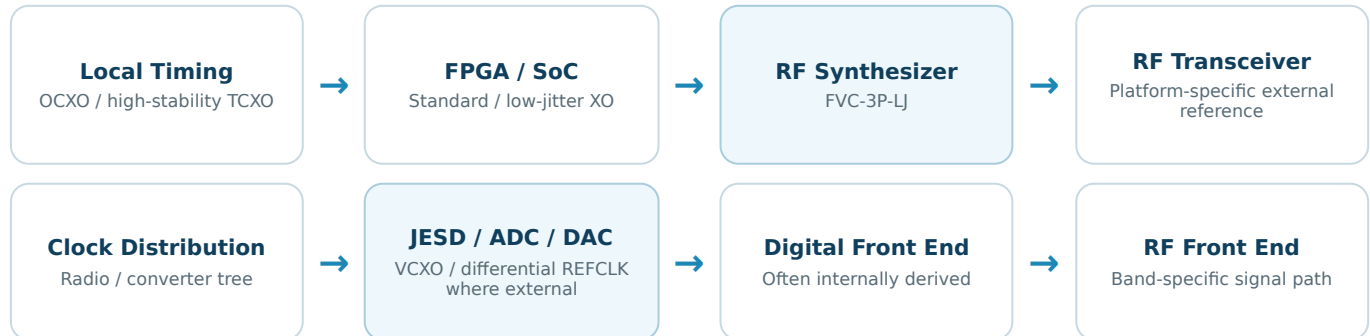


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RU / Small Cell Digital & RF Architecture

Representative radio-unit / small-cell architecture showing typical positions for FCom oscillator and filter families within digital, RF and optional IF signal paths.

Digital & RF Clock Path



RF Front-End Filtering



Selected Narrowband IF Path



Architecture-dependent: MCF crystal filters are primarily applicable to narrowband IF or specialized radio architectures. Their use is not typical across all wideband RAN platforms.

Position	Representative Frequency / Band	Representative FCom Series	Selection Relevance
FPGA / SerDes	100 / 125 / 156.25 MHz	FCO-3L-UJ	100–220 MHz · 50 fs · LVPECL / LVDS / HCSL · –40 to +125°C
RF Synthesizer / Transceiver	30.72 / 38.4 / 122.88 MHz	FVC-3P-LJ	Tunable CMOS reference up to 250 MHz; use only where PLL control / pullability is required.
JESD / Converter REFCLK	122.88 / 156.25 / 245.76 MHz	VCXO / Differential XO	Confirm first whether the converter clock is external; then select by jitter, phase noise and interface.
RF Front End	3.5 GHz-class example	FSF1411-3500M-200M-2-40	3500 MHz center · 200 MHz BW · 2 dB listed insertion loss · 40 dB listed attenuation. Final mask must be verified.
Narrowband IF	21.4 / 45 MHz examples	FCF-7M	Representative MCF family for narrowband IF only; bandwidth, insertion loss and termination remain configuration-specific.

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FCom Solutions by System Function

Representative FCom solutions are shown for the principal RAN timing, RF, digital and filtering functions. Exact device configuration depends on the target IC, interface and system-level performance requirements.

Precision Timing

OCXO / high-stability TCXO coverage for synchronization, DPLL and holdover nodes.

RF Reference

Fixed and tunable reference families for RF PLL, synthesizer and transceiver clock trees.

High-Speed Digital

Low-jitter differential XO coverage for eCPRI, Ethernet, FPGA and SerDes reference clocks.

RF / IF Filtering

Band-specific SAW and architecture-dependent MCF options; final passband and rejection mask govern selection.

System Function	Representative FCom Series	Key Catalog Specifications	Recommended Use
Precision Timing / Holdover	FOC-5S-LN	14x9 mm SMD · 10–40 MHz · 3.3 / 5 V · ±5 ppb · –40 to +85°C · –162 dBc/Hz @10 kHz listed phase noise.	GNSS-disciplined timing, DPLL local reference and holdover where OCXO performance is justified.
Compact / Outdoor Timing	FVT-7S-WT	7050 · 10–52 MHz · 2.5 / 3.3 V · ±50 ppb · –40 to +105°C · CMOS / clipped-sine options.	RU local timing and synchronized outdoor radio nodes where smaller size / lower power is preferred over OCXO holdover.
Tunable RF Reference	FVC-3P-LJ	3225 · 10–250 MHz · CMOS · ±50 to ±150 ppm pull range · –40 to +105°C.	RF PLL / synthesizer and selected 122.88 MHz-class reference nodes requiring tuning.
Low-Jitter Fronthaul / SerDes	FCO-3L-UJ	3225 · 100–220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · –40 to +125°C · 50 fs listed RMS jitter.	125 / 156.25 MHz eCPRI, Ethernet, FPGA and SerDes REFCLK.
Local Processor Clock	FCX-3M / FCO-3C	FCX-3M: 3225 crystal, 8–80 MHz, ±5 ppm tolerance / ±10 ppm stability. FCO-3C: 3225 CMOS XO, 1.25–125 MHz, ±20 ppm.	Choose passive crystal or active XO according to the MCU / SoC oscillator-input architecture.
RF / IF Filtering	FSF1411 family FCF-7M	SAW selection is band- and mask-specific. FCF-7M is applicable only to specialized narrowband IF architectures where crystal-filter selectivity is required.	RF front-end rejection and optional narrowband IF; never select from center frequency alone.

Part-number selection: crystal and oscillator series are configured according to frequency, supply, output, stability, temperature, control / OE and package requirements. SAW filters additionally require the complete RF passband and rejection mask. FCom can confirm the final ordering code after these parameters are defined.

ENGINEERING SELECTION SUPPORT

Request an FCom Device Recommendation

Send the target IC / module and clock pin together with frequency, output, supply, stability / jitter / phase-noise target, temperature and package. For filters, include center frequency, bandwidth and rejection mask.

[Start Engineering Review →](#)

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Engineering Validation & Selection Checklist

Confirm the complete electrical, timing and RF requirements before final component selection and production release.

Quartz Crystal

- Frequency, CL, ESR, C0 and drive level
- Initial tolerance and temperature stability
- Negative resistance and startup margin
- Verify that the target IC provides the oscillator circuit

Standard / Differential XO

- Supply voltage, LVDS / LVPECL / HCSL / CMOS input requirement
- Duty cycle, rise / fall time and OE behavior
- Termination, fan-out and signal integrity
- Jitter integration bandwidth and mask

TCXO / OCXO / VCXO

- Temperature stability, aging and warm-up / holdover
- Phase-noise offsets relevant to the RF / timing architecture
- VCXO pull range / APR and control voltage
- Confirm whether the receiving input expects sine, clipped-sine, CMOS or differential

SAW / MCF Filter

- Center frequency / band and passband
- Insertion loss, ripple and complete rejection mask
- Impedance / VSWR and power constraints
- Package, temperature and actual RF / IF placement

Minimum RFQ Information

Information Category	What to Provide
System / Clock Node	Equipment type, CU / DU / RU / small-cell position, target IC / module and exact clock pin / interface; identify external, recovered or internally derived clock.
Oscillator / TCXO / VCXO / OCXO	Frequency, supply, output, stability, temperature, jitter / phase-noise target, package, OE / control function, pullability and warm-up / holdover when applicable.
Quartz Crystal	Frequency, CL, ESR, C0, drive level, tolerance, temperature stability, package and oscillator-circuit information.
SAW Filter	Center frequency / band, bandwidth, insertion loss, ripple, full rejection mask, impedance, package, temperature and RF power level.
MCF Crystal Filter	Center frequency, 3 dB bandwidth, stopband requirement, insertion loss, ripple, terminating impedance, package and temperature.
Project / Program	Prototype quantity, sample date, qualification timing, annual volume, production site and any reliability / environmental constraints.

Timing Architecture

Selection depends on the GNSS / PTP / SyncE hierarchy, DPLL mode, holdover requirement, aging and phase-noise budget.

Digital Clock Tree

Confirm the receiving interface, differential logic, jitter integration bandwidth, fan-out and signal-integrity requirements.

RF / Filter Path

RF reference and filter selection must follow the target PLL / transceiver architecture and complete filter mask—not merely nominal frequency.

Frequency alone is not sufficient for final selection: a 156.25 MHz reference still requires confirmation of output logic, jitter requirements, supply and package, while a 3500 MHz SAW filter also requires bandwidth, insertion loss and the complete rejection mask. The final ordering code follows the complete electrical specification.

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Engineering FAQ & Application Review

Common selection questions, product interpretation and primary public technical references.

When is an OCXO justified in a RAN timing node?

Use an OCXO when holdover, long-term aging and tight frequency stability dominate the design. **FOC-5S-LN** is shown as a representative low-noise OCXO option for this class of timing node.

What should be checked for a 156.25 MHz eCPRI / SerDes REFCLK?

Confirm differential logic, RMS-jitter budget, supply, termination and temperature range. **FCO-3L-UJ** is shown as a representative 3225 low-jitter option for this REFCLK class.

What should be evaluated for a 122.88 MHz RF / converter reference?

First confirm that 122.88 MHz is an external reference. Then determine whether the node requires a fixed clock or tuning; **FVC-3P-LJ** is shown as a representative tunable CMOS VCXO option.

Does every internal RAN clock require a dedicated oscillator?

No. Sampling, processing and line-rate clocks are often generated by PLLs, DPLLs, FPGA clock trees or transceiver synthesizers. Select an external oscillator only for a documented reference input.

Can a SAW filter be selected from center frequency alone?

No. Bandwidth, insertion loss, ripple, rejection mask, impedance, package and temperature must all be evaluated. Full FCom SAW ordering codes are selected only after the RF mask is known.

Is an MCF crystal filter a standard RAN component?

No. MCF is retained only for narrowband IF or specialized radio architectures; it is not a universal component in modern wideband RAN systems.

Primary Technical References

1. **Microchip:** M.2 Timing Modules — synchronization / holdover architecture context.
2. **Analog Devices:** AN-2589 — ADRV904x clock tree, DEVCLK / SYSREF and 122.88 MHz VCXO context.
3. **Texas Instruments:** AFE79xx EVM — 10 MHz synchronization example and RF-sampling clock architecture.
4. **Altera:** O-RAN design example — 156.25 MHz Ethernet REFCLK and internally generated eCPRI / PTP domains.

FCom product specification note: product information in this guide is presented at the series or representative configuration level. Exact ordering codes, guaranteed limits and availability should be confirmed against the applicable FCom datasheet and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

Wireless RAN Timing & RF Application Review

Share the system position, target IC / module, required external frequency or RF band, performance limits, operating temperature, package constraints and project stage. FCom can review the requirement and recommend an appropriate product series and configuration.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection should be verified against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.