

TWS, HEADPHONES & PERSONAL AUDIO

TWS, Headphones & Personal Audio

This guide supports selection of external timing components for Bluetooth connectivity, digital audio processing, codec / DAC / ADC conversion and low-power standby in compact personal-audio platforms.

Wireless Reference + Audio Master Clock + Sleep / RTC + Conditional 2.4 GHz RF Filtering

TWS Earbuds

Bluetooth Headphones

IEM

Portable Audio Player

Portable DAC

Hearing Device

Wireless Personal Audio

Application Scope

Wireless and wired personal-audio products combining a Bluetooth SoC, host MCU or USB interface, DSP, codec, DAC / ADC, headphone driver and low-power control.

Selection Philosophy

Wireless Clock and Audio Clock are separate engineering domains. The radio reference is selected from the wireless IC oscillator interface; a dedicated audio XO is considered only when the codec, DAC, DSP or clock-control architecture exposes a suitable input.

Wireless Clock

Bluetooth / LE Audio SoC crystal or documented external clock.

Audio Clock

Low-jitter MCLK for DSP, codec, DAC or ADC where required.

RTC & Standby

Optional 32.768 kHz sleep, wake and retained-time reference.

Conditional RF

External 2.4 GHz SAW only at a documented RF insertion point.

TWS Priority

Minimize area and active current. Start with the wireless SoC crystal and use internal audio-clock generation where it meets the system requirement.

Portable Hi-Fi Priority

Separate system timing from the audio MCLK and evaluate jitter, phase noise, supply noise and sample-rate switching at the receiving pin.

Hearing-Device Priority

Balance low-power standby, fast wake, compact packaging and stable wireless operation across defined operating states.

01

Application Scope & Engineering Domains

Personal-audio platforms may combine radio, DSP and conversion clocks inside one SoC or distribute them across several devices.

Separate the clock domains before selecting a component. A Bluetooth crystal establishes the wireless / system reference. An audio master clock controls conversion timing only when the codec, DAC, ADC or DSP architecture provides a dedicated MCLK or clock-input node.

Typical Equipment

Ultra-Compact Wireless

TWS Earbud
Bluetooth Headphone
Wireless IEM
Hearing Device
Charging-Case Controller

Portable Hi-Fi

Digital Audio Player
Portable DAC / Amp
USB Audio Interface
Wireless DAC
High-Resolution Headphone

Voice & Assistive Audio

Voice Headset
Conference Headset
Hearable Sensor Platform
Assistive Listening Device
Personal Audio Transmitter

Six Engineering Domains

Bluetooth Reference

Chip-down wireless SoC crystal or documented CLKIN.

Host / USB / DSP

System crystal feeding MCU, USB bridge or processing PLL.

Codec / DAC / ADC

44.1 kHz-family or 48 kHz-family audio MCLK.

Clock Control

Selector, PLL, ASRC or controlled-pull reference.

Sleep / RTC

Optional always-on low-frequency domain.

RF Front End

Conditional 2.4 GHz coexistence or blocking filter.

Physical Interface

XTAL pins · CMOS CLKIN · clipped-sine input · module-internal clock.

Clock Quality

Radio ppm · RMS jitter band · phase-noise offsets · pulling range.

Power & Size

Startup · active current · sleep strategy · 1210 / 2016 placement.

Architecture Boundary

Chip-down IC · wireless module · integrated codec · discrete audio clock.

Wireless-Clock Decision

Use a passive crystal at supported oscillator pins. Use a driven source only where the radio or host documents external-clock mode.

Audio-Clock Decision

Confirm whether MCLK is internal, shared, PLL-derived or externally driven before assigning a low-jitter XO.

Module-Boundary Decision

A host-PCB clock position is normally unnecessary when the wireless or audio module already integrates its required reference.

Clock-definition note: audio sample rate, BCLK, LRCK and the Bluetooth 2.4 GHz carrier are not automatically external oscillator frequencies. Select the external timing source from the receiving IC clock-input specification.

02

Select by System Node First

Begin with the receiving clock pins, then determine whether the project needs a passive resonator, driven clock, controlled-pull source or no external device.

System Node	Clock Role	Representative External Reference	Typical Device	Selection Focus
Sleep / RTC	Wake scheduling and retained time	32.768 kHz	Tuning-fork crystal / low-current XO	XTAL vs CLKIN · CL · ESR · current · drift
Chip-Down Bluetooth Audio SoC	Radio and baseband reference	16 MHz on selected platforms	MHz crystal	specified tolerance · CL · ESR · startup
Host / USB / Wireless System	System / PLL reference	24 MHz class	MHz crystal / CMOS clock	receiver mode · CL / ESR or VDD / logic
LE Audio / Wireless SoC	Radio and system reference	32 MHz	Miniature MHz crystal	radio ppm · negative resistance · package
44.1 kHz Audio Family	Codec / DAC / ADC master clock	11.2896 / 22.5792 / 45.1584 MHz	Low-jitter CMOS XO / controlled clock	exact MCLK ratio · jitter band · current
48 kHz Audio Family	Codec / DAC / ADC master clock	12.288 / 24.576 / 49.152 MHz	Low-jitter CMOS XO / controlled clock	exact MCLK ratio · jitter band · switching
Wireless Module	Module-internal reference	Usually integrated	Internal crystal / oscillator	confirm whether host REFCLK is exposed
External 2.4 GHz RF Node	Coexistence / out-of-band selectivity	2437 / 2442 MHz class	SAW filter	passband · loss · impedance · attenuation mask

1 · Identify the Receiver

Record the exact Bluetooth SoC, host MCU, DSP, codec, DAC, ADC, clock IC or module and the clock pins used by the design.

2 · Establish the Boundary

Determine whether the clock is customer-selectable, generated internally, already integrated in a module or provided by another IC.

3 · Apply Electrical Constraints

Define CL / ESR for crystals; VDD, logic and load for XOs; jitter and phase-noise criteria for audio; and the full mask for RF filters.

Recommended sequence: System node → physical interface → frequency → device class → accuracy / jitter / phase noise → power / startup → temperature → package → FCom application review.

Wireless SoC Has XTAL Pins

Select a passive MHz crystal from the documented frequency, CL, ESR, drive-level and radio-accuracy budget.
Representative FCom family: FCX miniature crystals

Audio Device Has Dedicated MCLK

Evaluate a CMOS XO only after the exact audio family, MCLK ratio, VDD, loading and jitter measurement band are defined.
Representative FCom families: low-jitter / programmable XO

Clock Is Integrated or Internally Derived

No additional external timing device is normally required at that node. Selection can therefore focus on the remaining customer-selectable wireless, RTC or RF positions.
Selection outcome: no external component required

Selection boundary: when the receiver datasheet, module hardware guide or schematic does not expose a selectable clock input, frequency similarity alone is insufficient grounds for adding a component.

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Frequency & Component Placement Matrix

Wireless, system, audio and RF-filter frequencies can coexist in one product but serve different electrical functions.

Frequency	Representative System Position	Applicability	Selection Interpretation
32.768 kHz	Sleep timer, RTC, wake controller, charging case	Optional Low-Power Domain	Use a passive tuning-fork crystal for XTAL pins or a low-current XO for a documented driven-clock input.
16 MHz	Selected chip-down Bluetooth audio SoC	Platform-Specific Wireless	External passive crystal where the SoC specifies a 16 MHz oscillator loop; a module implementation may integrate it.
24 MHz	USB audio controller, host MCU, DSP / system reference	Common System Reference	Normally a passive crystal or driven clock at the documented system input; higher core clocks are synthesized internally.
32 MHz	Bluetooth LE / LE Audio wireless SoC	Common Wireless Reference	Miniature crystal at HFXO pins on chip-down designs; no host-PCB replacement when already integrated in a module.
11.2896 / 22.5792 / 45.1584 MHz	44.1 / 88.2 / 176.4 kHz-family audio MCLK	Dedicated Audio Clock	Select only when a codec, DAC, ADC, DSP or clock IC exposes the matching MCLK ratio and electrical input.
12.288 / 24.576 / 49.152 MHz	48 / 96 / 192 kHz-family audio MCLK	Dedicated Audio Clock	May be generated from a PLL or supplied by an external low-jitter XO; confirm the complete clock tree and switching strategy.
2437 / 2442 MHz class	External 2.4 GHz receive / coexistence filter position	RF Filter — Not a Clock	Center frequency and bandwidth are RF parameters; use is conditional on the radio reference design, matching and required mask.

Wireless

16 / 24 / 32 MHz according to the chip-down radio or host interface.

44.1 kHz Family

11.2896 / 22.5792 / 45.1584 MHz audio MCLK options.

48 kHz Family

12.288 / 24.576 / 49.152 MHz audio MCLK options.

Standby / RF

32.768 kHz timing; 2.4 GHz conditional RF filtering.

Frequency Match

The selected FCom series must cover the exact frequency—not only the general application family. This is why 16 MHz and 24 / 32 MHz may use different miniature-crystal series.

Electrical Match

A valid frequency is not sufficient. Passive-crystal CL / ESR and active-clock VDD / waveform / load must match the receiver.

Performance Match

Wireless accuracy, audio jitter, phase noise and controlled pull are different specifications and should not be treated as substitutes.

Frequency interpretation: 44.1 / 48 / 96 / 192 kHz are audio sample rates, while BCLK and LRCK are digital-interface clocks. The external oscillator frequency is the MCLK or reference explicitly required by the receiving device.

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Representative Platform & Architecture Matrix

Four public platforms illustrate wireless-only timing, module integration, separated wireless / audio clocks and dedicated high-performance audio timing.

NORDIC SEMICONDUCTOR

nRF5340 Audio DK · LE Audio / TWS / Auracast

1

Architecture: nRF5340 wireless SoC, audio DSP functions and a CS47L63 audio codec support LE Audio development and headset / earbud evaluation.

Timing evidence: the SoC uses a 32 MHz high-frequency crystal; 32.768 kHz is optional. The audio clock domain can be generated internally around the 44.1 / 48 kHz families.

32 MHz HFXO → nRF5340 → Codec / Audio

Engineering interpretation: the 32 MHz crystal is a custom-PCB selection point. An external audio XO should be evaluated only if the transferred design exposes and requires a dedicated audio-clock input.

MICROCHIP

IS2083BM / BM83 · Bluetooth Stereo Audio

2

Architecture: chip-down IS2083 and module-based BM83 implementations combine Bluetooth audio, DSP and digital-audio interfaces for headsets, speakers and portable audio.

Timing evidence: the chip-down IS2083 design specifies a 16 MHz external crystal with a ± 10 ppm requirement; the BM83 module integrates the crystal and DSP.

16 MHz XTAL → IS2083BM → I²S / Codec

Engineering interpretation: 16 MHz is relevant to the chip-down oscillator loop. It is not a host-board replacement for the crystal already integrated inside BM83.

NXP SEMICONDUCTORS

NxH3670 SDK · Low-Latency Wireless Audio

3

Architecture: the SDK separates host processing, the NxH3670 wireless IC and a WM8904 codec, making clock-domain boundaries visible.

Timing evidence: public board material identifies 24.576 MHz at the MKL27 host, 32 MHz at NxH3670 and a 12.288 MHz TCXO for the codec path.

24.576 MHz Host → 32 MHz Radio → 12.288 MHz Audio

Engineering interpretation: the platform demonstrates why host, wireless and audio clocks must be selected as separate nodes rather than consolidated by frequency alone.

XMOS

XK-AUDIO-316-MC-AB / XU316 · USB Audio

4

Architecture: a USB audio controller, multichannel digital audio and external codec / DAC interfaces provide a representative portable-DAC or high-performance audio clock tree.

Timing evidence: the board uses a 24 MHz system crystal and supports 22.5792 / 24.576 MHz audio-master-clock families for 44.1 / 48 kHz sample-rate groups.

24 MHz System → XU316 / USB → Audio MCLK

Engineering interpretation: a dedicated audio XO is relevant only when the final clock architecture assigns it to an exposed MCLK input; development-board population should not be treated as a universal production BOM.

Platform-use boundary: references to third-party platforms are provided solely to illustrate clock insertion points and architecture boundaries. They do not imply that FCom products are used, approved, qualified, endorsed or pin-compatible with the cited platforms.

Nordic

Wireless crystal plus internally managed audio timing.

Microchip

Chip-down 16 MHz opportunity versus module integration.

NXP

Explicitly separated host, radio and codec references.

XMOS

System crystal separated from audio MCLK families.

Chip-Down Wireless SoC

The external crystal is a genuine selection point when oscillator pins, load capacitance, ESR and accuracy limits are documented.

Selection basis: receiving oscillator-loop requirements

Integrated Wireless Module

The internal crystal is part of the module implementation. A host-board replacement should be considered only when a REFCLK input is documented.

Maintain the documented module boundary

Dedicated Audio Clock Input

An audio XO or controlled clock is evaluated only when the codec, DAC, ADC, DSP or selector exposes the node and its requirements.

Select by MCLK family and clock quality

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Compact TWS / LE Audio Timing Architecture

A power-first architecture in which the wireless reference is external, while the audio clock is generated internally unless the codec explicitly requires a separate source.



NODE 1 Wireless Crystal

24 / 32 MHz XTAL pins

For compact chip-down wireless SoCs whose oscillator loop accepts the selected frequency.

Selection checks

CL · ESR · tolerance / stability · drive level · negative resistance · startup.

Representative FCom option

FCX-1S

— 1210 4-SMD; 24–76.8 MHz; tolerance options down to ± 5 ppm; stability options down to ± 10 ppm; -40 to $+125^{\circ}\text{C}$; CL 18 pF or specified; ESR 60–100 Ω .

NODE 2 16 MHz Wireless

Selected Bluetooth SoC

Used only where the receiving oscillator loop explicitly specifies 16 MHz.

Why a separate series

The 1210 FCX-1S range begins at 24 MHz; the 16 MHz node therefore requires a different frequency-range option.

Representative FCom option

FCX-2S

— 2016 4-SMD; 16–96 MHz; tolerance options down to ± 5 ppm; stability options down to ± 10 ppm; -40 to $+125^{\circ}\text{C}$; CL 18 pF or specified; ESR 30–100 Ω .

NODE 3 Sleep / RTC

Optional 32.768 kHz domain

Use only where the SoC, PMIC, charging-case MCU or RTC exposes a selectable low-frequency input.

Passive vs driven

FCT-1S suits XTAL pins; FCO-6K-UC is considered only for a supported 1.5 / 1.8 V CMOS CLKIN.

Representative FCom options

FCT-1S

— 1210, ± 5 ppm option, -40 to $+125^{\circ}\text{C}$, CL 6–12.5 pF, ESR 70–90 k Ω .

FCO-6K-UC

— 2016, ± 20 ppm, 1.4–1.8 μA .

RF PATH Conditional SAW

External filter condition

Evaluate only when the 2.4 GHz radio front end exposes a filter location and a complete attenuation mask.

Published filter data

2442 MHz center · 79 MHz bandwidth · 1.2 dB insertion loss · 40 dB stopband attenuation.

Representative complete FCom P/N

FSF1109-2442M-79M-1.2-40

— CSP1109 SMD. Final suitability requires validation of impedance, matching, RF power and system coexistence.

Typical TWS Timing BOM

Wireless reference crystal; optional RTC only when its pins and standby requirement exist.

When to Evaluate an Audio XO

A dedicated XO is appropriate when an exposed MCLK input and measurable system benefit justify its power and area.

When to Evaluate a SAW Filter

Evaluation begins from a defined RF insertion point, mask, impedance and coexistence requirement.

Architecture guidance: a discrete audio XO is not a default requirement in a TWS earbud. When the Bluetooth SoC or codec can generate a compliant audio clock internally, a dedicated XO adds current and area and should therefore be justified by a defined system-level benefit.

06

Portable DAC / High-Performance Audio Clock Architecture

A separated system-clock and audio-master-clock design for portable players, USB DACs, wireless DACs and premium headphone platforms.



System Reference

A 24 MHz crystal can feed the USB controller or host PLL. It is separate from the audio sample-rate family even when 24.576 MHz appears elsewhere in the system.

Representative FCom path: FCX-15 where the receiver uses XTAL pins.

Dedicated Audio MCLK

Use 22.5792 / 24.576 MHz or 45.1584 / 49.152 MHz when required by the codec, DAC, ADC, DSP or clock selector.

Selection path: a low-jitter CMOS XO at the exact required frequency.

Controlled Pull

A VCTCXO is considered only when a control loop must trim the audio reference. Pull range, loop dynamics and receiver waveform remain system requirements.

Representative FCom path: FVT-5S in a supported VCTCXO configuration.

AUDIO XO Compact XO

Selection role

Flexible exact audio MCLK for development, multiple product variants or a clock selector accepting CMOS.

Published capability

2016 4-SMD · 1–200 MHz · 1.8 / 2.5 / 3.3 V · ± 15 ppm · –40 to +125°C · CMOS · 0.8 ps.

Representative FCom option FCO-6P-PJ

. Confirm the required frequency, load, enable behavior, phase-noise profile, jitter integration band and 25–40 mA published current range.

AUDIO XO Lower Published Jitter

Selection role

Dedicated single-ended audio clock where a larger package and active-current budget are acceptable.

Published capability

5032 6-SMD · 10–250 MHz · 2.5 / 3.3 V · ± 25 ppm · –40 to +85°C · CMOS · 0.6 ps · 30 mA.

Representative FCom option FCO-5P-UJ

. Use the published jitter only with its stated measurement conditions; validate at the DAC / codec input and analog output.

PULL / TRIM Conditional VCTCXO

Selection role

Frequency-tracking or disciplined-clock loop that requires limited electronic pull rather than a fixed XO.

Published capability

5032 4-SMD · 10–52 MHz · 1.8–3.3 V · stability option down to ± 0.5 ppm · CMOS / clipped sine · ± 5 ppm pull.

Representative FCom option FVT-5S

in a supported VCTCXO configuration; published phase-noise references are –115 / –135 / –148 dBc/Hz at 100 Hz / 1 kHz / 10 kHz.

Fixed Single Source

Best where one audio family is required and a dedicated low-jitter MCLK directly serves the receiver.

Dual-Family Source

Use a selector or defined switching sequence when separate 44.1 kHz- and 48 kHz-family clocks are fitted.

Controlled Source

Use a VCTCXO only with a documented trim loop; stability and pull do not replace jitter verification.

Audio-quality rule: RMS jitter values are comparable only when the integration band, carrier frequency, output loading and measurement method are known. Final selection is verified at the receiving clock pin and through the complete audio signal path.

07

FCom Selection Guidance by Design Condition

Only options that create a clear architectural or specification choice are shown. Final ordering codes are confirmed after the receiver interface and exact frequency are reviewed.

Wireless XTAL

Compact passive reference selected from the chip-down radio oscillator loop.

Audio MCLK

Dedicated CMOS XO only when the audio clock input and power budget support it.

RTC / Standby

Optional passive or driven 32.768 kHz source.

Conditional RF

External 2.4 GHz SAW at a documented front-end insertion point.

Design Condition	Representative FCom Option	Published Capability / Application Rationale	Key Check Before RFQ
Optional 32.768 kHz XTAL pins + minimum area	FCT-1S	1210 2-SMD; 32.768 kHz; tolerance options down to ± 5 ppm; -40 to $+125^{\circ}\text{C}$; CL 6–12.5 pF; ESR 70–90 k Ω .	XTAL mode · CL · ESR · drive · startup
24 / 32 MHz wireless XTAL + minimum area	FCX-1S	1210 4-SMD; 24–76.8 MHz; tolerance options down to ± 5 ppm; stability options down to ± 10 ppm; -40 to $+125^{\circ}\text{C}$; CL 18 pF or specified; ESR 60–100 Ω .	frequency · CL · ESR · negative resistance
16 MHz wireless XTAL	FCX-2S	2016 4-SMD; 16–96 MHz; tolerance options down to ± 5 ppm; stability options down to ± 10 ppm; -40 to $+125^{\circ}\text{C}$; CL 18 pF or specified; ESR 30–100 Ω .	± 10 ppm system budget · drive · startup
Compact programmable CMOS audio MCLK	FCO-6P-PJ	2016 4-SMD; 1–200 MHz; 1.8 / 2.5 / 3.3 V; ± 15 ppm; -40 to $+125^{\circ}\text{C}$; CMOS; 0.8 ps published jitter; 25–40 mA.	exact frequency · integration band · load · current
Dedicated CMOS audio MCLK + lower published jitter	FCO-5P-UJ	5032 6-SMD; 10–250 MHz; 2.5 / 3.3 V; ± 25 ppm; -40 to $+85^{\circ}\text{C}$; CMOS; 0.6 ps published jitter; 30 mA.	size · power · jitter method · phase-noise profile
Audio-control loop requires limited electronic pull	FVT-5S VCTCXO configuration	5032 4-SMD; 10–52 MHz; 1.8–3.3 V; stability options down to ± 0.5 ppm; CMOS / clipped sine; ± 5 ppm pull; published phase-noise reference values.	pull law · control voltage · waveform · loop bandwidth
Documented external 2.4 GHz filter position	FSF1109-2442M-79M-1.2-40	Complete FCom P/N; CSP1109 SMD; 2442 MHz center; 79 MHz bandwidth; 1.2 dB insertion loss; 40 dB stopband attenuation.	mask · impedance · matching · RF power · coexistence

Ordering information: FCT, FCX, FCO and FVT are shown at series level because the complete ordering code depends on frequency and configuration details such as CL, tolerance / stability, voltage, output and option suffixes. FCom confirms the complete code against the applicable specification during application review and quotation. The SAW entry is a complete part number and remains subject to RF validation.

ENGINEERING SELECTION SUPPORT

Request an FCom Personal-Audio Timing Review

Provide the target wireless SoC, MCU / USB controller, DSP, codec / DAC / ADC or module, together with the clock pins, frequency, CL / ESR or supply / waveform, audio sample-rate family, jitter criteria, power budget, package and project stage.

[Start Engineering Review →](#)

08

Engineering Validation & Minimum RFQ

Personal-audio clock selection is defined by the receiving interface, sample-rate architecture, power state and measurement conditions in addition to frequency.

Wireless / System Crystal

- Exact SoC / MCU part number
- 16 / 24 / 32 MHz oscillator pins
- CL, ESR and negative-resistance margin
- tolerance / stability and startup limit
- module or chip-down implementation

Dedicated Audio Clock

- Codec / DAC / ADC / DSP clock input
- 44.1 kHz or 48 kHz sample-rate family
- MCLK frequency and ratio
- VDD, logic, load and enable state
- RMS jitter band and phase-noise mask

Sleep / RTC

- XTAL pins or driven CLKIN
- 32.768 kHz CL / ESR or VDD / current
- standby supply domain
- wake latency and startup
- retained-time drift requirement

External RF Filtering

- Antenna / switch / LNA / PA topology
- full 2.4 GHz passband and stopband mask
- insertion loss and port impedance
- matching network and RF power
- coexistence interferers and temperature

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Wireless SoC, host / USB controller, DSP, codec, DAC, ADC, RTC or external RF-filter location.
Target Device	Exact receiving IC or module part number, schematic clock pins and whether the source is customer-selectable.
Frequency Architecture	System reference, audio MCLK family, clock-divider / PLL / ASRC plan and supported power / sample-rate states.
Crystal Requirements	Frequency, package, CL, ESR, tolerance / stability, drive level, negative resistance, startup and temperature.
Oscillator / VCTCXO Requirements	Frequency, VDD, waveform, load, current, OE, pull range, control voltage, RMS jitter integration band and phase-noise offsets.
Program Requirements	Prototype quantity, sample date, annual volume, validation plan, manufacturing location, lifecycle and compliance documentation.

XTAL vs CLKIN

A passive resonator and a driven oscillator are different source types and cannot be interchanged without a supported bypass mode.

44.1 vs 48 kHz Family

Define whether the design switches between two MCLK families, uses a PLL / ASRC or accepts one fixed reference.

Chip-Down vs Module

A chip-down design may expose crystal pins while the equivalent module integrates the reference internally.

Frequency alone does not define the final part: the receiver mode, clock-tree topology, power budget, jitter measurement conditions, module boundary and RF architecture determine the FCom series and configuration to evaluate.

09

Engineering FAQ & Application Review

Common personal-audio timing questions, representative public references and the information required for FCom engineering review.

Does Bluetooth at 2.4 GHz require a 2.4 GHz oscillator?

No. The carrier is synthesized from a lower-frequency reference. A 2.4 GHz SAW, when present, is an RF filter.

Is the audio sample rate the external oscillator frequency?

No. 44.1 / 48 / 96 / 192 kHz are sample rates. The external source may be an MCLK such as 22.5792 or 24.576 MHz.

Does every TWS earbud need a dedicated audio XO?

No. Many wireless SoCs or codecs generate the audio clock internally. A discrete XO is used only when an exposed clock input and system benefit are established.

Can one XO support both audio sample-rate families?

Only if the clock selector, PLL or ASRC architecture supports it. Otherwise separate 44.1 kHz- and 48 kHz-family MCLKs may be required.

Can a CMOS XO replace a passive crystal?

Only when the receiving device provides a supported external-clock or bypass mode with compatible voltage and waveform limits.

Can a module-internal crystal be replaced on the host PCB?

Normally no. A host timing opportunity exists only if the module exposes a documented reference-clock input.

When is a VCTCXO appropriate in audio?

When a defined control loop must trim the reference. Pull range, control law, loop bandwidth and output waveform must be specified.

When should an external 2.4 GHz SAW be considered?

Only when the RF front end exposes a filter location and the passband, loss, impedance, attenuation and RF-power requirements are defined.

Representative Public Technical References

- Nordic Semiconductor:** nRF5340 Audio DK — LE Audio / TWS / Auracast development platform.
- Nordic Semiconductor:** nRF5340 oscillator specifications — 32 MHz HF XO and low-frequency clock options.
- Microchip:** IS2083BM clocking — 16 MHz external crystal requirement for chip-down implementation.
- Microchip:** BM83 architecture — module-integrated Bluetooth audio, DSP and crystal boundary.
- NXP Semiconductors:** NxH3670 SDK board — separated host, wireless and codec clock domains.
- XMOS:** XK-AUDIO-316-MC-AB hardware manual — 24 MHz system and audio-clock architecture.
- XMOS:** XU316 datasheet — system-clock and xCORE audio processing interface.
- FCom Fuji Crystal:** product information and application-engineering contact for timing and RF component review.

FCom product specification note: product information in this guide is presented at series or representative-configuration level unless a complete SAW part number is shown. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom specification and quotation.

ENGINEERING REVIEW

TWS, Headphones & Personal Audio Review

Provide the target wireless SoC, host / USB controller, DSP, codec / DAC / ADC or module, together with clock pins, frequency, CL / ESR or supply / waveform, sample-rate family, jitter criteria, power budget, package and project stage. FCom application engineering can evaluate suitable options for board-level validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system. Audio performance, RF coexistence, EMC, battery life and regulatory compliance remain system-level responsibilities of the equipment manufacturer.