

TIMING INFRASTRUCTURE & CRITICAL NETWORKS

Timing Infrastructure & Critical Networks

Support resilient time, frequency and phase continuity during source degradation, reference loss and network faults across telecom, energy, finance, industrial and other critical-infrastructure networks.

Trusted Reference + Source Protection + Local Holdover + Resilient Distribution + Platform Clocking

ePRTC / PRTC

PTP / IEEE 1588

SyncE

10 MHz / 1PPS

IRIG-B

White Rabbit

Application Scope

Primary clocks, grandmasters, time servers, SSU / BITS equipment, substation clocks, financial UTC service nodes, industrial timing systems and high-speed platform-clock domains.

Selection Philosophy

Selection begins with the clock node and permitted time error. Holdover, DPLL reference and high-speed REFCLK positions are separate timing domains even when they coexist in one appliance.

Trusted Source

GNSS, UTC(k), upstream PTP and external 10 MHz / 1PPS acquisition.

Local Holdover

OCXO / TCXO continuity during reference loss or degradation.

Network Distribution

PTP, SyncE, NTP, White Rabbit, IRIG and legacy timing I/O.

Platform Clocking

Ethernet, PCIe, FPGA, SerDes and optical-interface references.

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Application Scope & Engineering Domains

Critical-network timing combines trusted-reference acquisition, local timescale maintenance, resilient distribution and equipment-level clocking.

One timing appliance, multiple clock roles. A high-stability 10 MHz holdover oscillator, a pullable DPLL reference and a low-jitter 156.25 MHz platform clock solve different engineering problems. Each device should be selected for the receiving node and its specific performance budget.

Typical Equipment

Telecom & Network Timing
ePRTC / PRTC
Grandmaster Clock
SSU / BITS
Boundary Clock
Timing Service Node

Energy & Critical Infrastructure
Substation Clock
Grid Monitoring
Public-Safety Timing
Industrial Time Server
Multi-Site Facility

Financial & Platform Timing
UTC Service Node
Trading Timestamping
Data Center Endpoint
Ethernet / PCIe Clocking
Optical / SerDes REFCLK

Five Engineering Domains

Reference Acquisition
GNSS, UTC(k), PTP and external frequency / phase inputs.

Qualification & Servo
Priority, monitoring, switching, filtering and local timescale control.

Local Holdover
OCXO / TCXO performance during loss or rejection of the reference.

Network Distribution
Packet, physical-layer, legacy timing I/O and redundant paths.

Equipment Clocking
Processor, Ethernet, PCIe, FPGA, SerDes, optical and RTC references.

Time-Error Budget
Allowed phase / time error, outage duration, recovery and re-lock limits.

Stability & Noise
Initial accuracy, temperature, aging, retrace, phase noise and jitter.

Clock Interface
CMOS, clipped sine, LVDS, LVPECL, HCSL, 1PPS and passive XTAL inputs.

Critical Environment
Temperature, supply noise, airflow, vibration, lifecycle and validation.

Clock-definition note: PTP, NTP, SyncE and White Rabbit describe system-level timing transport. They do not by themselves define the local oscillator. The oscillator class follows the servo architecture, outage target, receiving interface and environmental conditions.

02

Select by System Node First

Identify the clock position, permitted outage-time error and receiving interface before comparing oscillator families.

System Node	Clock Role	Representative Signals / Frequencies	Typical Device	Selection Focus
ePRTC / PRTC / Grandmaster	Trusted source and extended holdover	10 MHz GNSS / UTC(k) · 1PPS / ToD · PTP	Low-aging OCXO	time error · outage · aging · retrace · warm-up · phase noise
Telecom DPLL / SSU / BITS	Reference filtering, synthesis and switching	10 / 19.44 / 20 / 25 / 30.72 / 38.4 / 38.88 MHz	TCXO / OCXO / VCXO	pull range · loop bandwidth · slope · wander · holdover estimator
Power Substation Clock	Relay, PMU, IED and sampled-value alignment	10 MHz · 1PPS · IRIG-B PTP power profiles	OCXO / TCXO	24 h time error · PRP · cable delay · redundant power · temperature
Financial UTC Service Node	Traceability, continuity and audit support	Traceable PTP local 10 MHz / 1PPS as required	OCXO + service monitoring	point-of-use accuracy · calibration · asymmetry · loss-of-feed behavior
Industrial / Public-Safety Time Server	Multi-format distribution and failover	GNSS · PTP / NTP · 10 MHz · 1PPS · IRIG	OCXO / high-stability TCXO	source priority · security · dual-site resilience · alarm policy
Ethernet / PCIe Platform Clock	PHY, switch ASIC, processor and PCIe reference	25 / 50 / 62.5 / 100 / 125 MHz	CMOS / differential XO	output logic · termination · SSC · additive jitter · integration band
Optical / SerDes REFCLK	OTN, FPGA, DSP and optical-interface reference	155.52 / 156.25 / 312.5 / 622.08 MHz	Low-jitter differential XO	device jitter mask · phase-noise floor · spurs · output swing
RTC / Supervisory Controller	Boot, logs and low-power housekeeping	32.768 kHz local 20 / 25 / 40 / 50 MHz	Crystal / low-current XO	XTAL vs CLKIN · CL · ESR · current; not a holdover source

1 · Define the Clock Role

Identify whether the device is a trusted source, holdover oscillator, DPLL reference, fixed REFCLK or RTC reference.

2 · Quantify the Performance Budget

Specify permitted time error, outage duration, aging, temperature, phase-noise mask or RMS-jitter band.

3 · Apply Interface Constraints

Confirm frequency, VDD, output logic, load, pull range, package, temperature and target-device clock topology.

Recommended sequence: System node → clock role → time-error / jitter budget → frequency → device class → electrical interface → environment → final FCom configuration.

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Frequency & Component Placement Matrix

Frequency becomes meaningful only when it is tied to the timing node, clock role and receiving interface.

Frequency	Representative System Position	Applicability	Selection Interpretation
32.768 kHz	RTC, supervisor and low-power controller	Retained-Time Reference	Tuning-fork crystal or low-current XO according to the target IC; this node should not be treated as a network holdover source.
1.544 / 2.048 MHz	T1 / E1 and legacy BITS / SSU output	Legacy Distribution	Normally synthesized by the timing DPLL. Confirm G.703 interface, wander and whether the signal is data-bearing.
10 MHz	PRTC / ePRTC, grandmaster, time server and external reference	Primary Holdover Anchor	Calculate time error from initial offset, temperature, aging, retrace, supply and outage duration.
19.2 / 19.44 / 20 MHz	GNSS / SoC, SONET / SDH and DPLL input	Platform-Dependent	19.2 and 19.44 MHz are not interchangeable. Confirm the exact clock plan and pullability requirement.
25 / 50 / 62.5 MHz	Ethernet PHY, controller and clock generator	Board-Level Reference	May be local, shared, forwarded or synthesized. Confirm source direction, logic, load and OE behavior.
30.72 / 38.4 / 38.88 MHz	Telecom DPLL, transport timing and synchronization card	Precision Sync Reference	38.4 and 38.88 MHz belong to different clock families. Check stability, slope, phase noise and free-run behavior.
100 / 125 MHz	PCIe, Ethernet PHY, switch ASIC and NIC	High-Speed Platform Clock	Output logic and target-device jitter band take priority over nominal frequency alone.
155.52 / 156.25 MHz	SONET / SDH, Ethernet SerDes, FPGA and optical modules	Low-Jitter Differential	The two frequencies are not substitutes. Confirm line architecture, logic swing, termination and device mask.
312.5 / 622.08 MHz	High-speed SerDes, OTN / DSP, FPGA and optical line card	High-Frequency REFCLK	Validate phase-noise floor, spurs and integration band. Treat this clock as a platform reference, not a UTC holdover source.

10 MHz Primary local frequency and quantified holdover domain.	30.72 / 38.4 / 38.88 Telecom DPLL fixed or pullable local-reference domain.	100 / 125 / 156.25 Ethernet, PCIe and SerDes low-jitter reference layer.	312.5 / 622.08 High-frequency optical, OTN, DSP and FPGA REFCLK layer.
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Reference-clock interpretation: protocol name, data rate and nominal frequency do not define the oscillator by themselves. Final selection should be based on the receiving IC clock specification, system clock tree and required performance mask.

04

Representative Platform & Architecture Matrix

Four public platforms illustrate protected telecom timing, substation resilience, financial UTC traceability and dual-site critical-facility distribution.

MICROCHIP

1

TimeProvider 4100 + TimeCesium + XT · Telecom Timing Backbone

Architecture: protected GNSS or UTC(k) references are centralized at core sites, with redundant east-west timing flows toward aggregation and legacy timing fan-out.

Public evidence: Microchip publishes a 30 ns ePRTC source, a 100 ns aggregation architecture and up to 40 days of holdover in the ePRTC / cesium configuration.

GNSS / UTC(k)

→

ePRTC + Cesium

→

PTP / SyncE / Legacy

Selection insight: core holdover and packet / legacy fan-out are separate layers; the local OCXO is typically evaluated at the protected continuity node.

SCHWEITZER ENGINEERING LABORATORIES

2

SEL-2488 · Satellite-Synchronized Substation Network Clock

Architecture: satellite / PTP references, selectable local oscillator grades and PRP-capable network distribution support protection and automation systems.

Public evidence: SEL publishes IRIG-B / 1PPS accuracy of ±40 ns average, PTP ±100 ns peak, and 24 h holdover of 315 µs TCXO, 5 µs OCXO and 2.5 µs DOCXO.

GPS / PTP

→

TCXO / OCXO / DOCXO

→

PRP / IRIG / 1PPS

Selection insight: the permitted 24-hour time error is a primary factor in determining oscillator grade; PRP and power-profile behavior remain system functions.

NPL / UBS

3

NPLTime Certified · GNSS-Independent Financial UTC Service

Architecture: UTC(NPL) is distributed through redundant fiber PTP feeds to monitored service nodes with local steered cesium holdover.

Public evidence: NPL publishes ±1 µs to UTC at reseller locations, 99.9% uptime and up to 30 days of service-node holdover after total PTP loss.

UTC(NPL) + Masers

→

Dual PTP + Cesium

→

Certified Service PoP

Selection insight: a local oscillator supports continuity, while UTC traceability, calibration and monitoring remain service-level requirements.

SAFRAN

4

SecureSync 2400 + WROX · Dual-Site Critical Facilities

Architecture: multi-GNSS acquisition, selectable internal oscillators, modular outputs and dual-site White Rabbit / PTP backup operate over 1 or 10 GbE.

Public evidence: published 24 h typical drift is 450 µs TCXO, 25 µs OCXO, 10 µs low-noise OCXO and 1 µs rubidium, with holdover derived from the internal 10 MHz oscillator.

Site A GNSS

↔

SecureSync + WR

↔

Site B GNSS

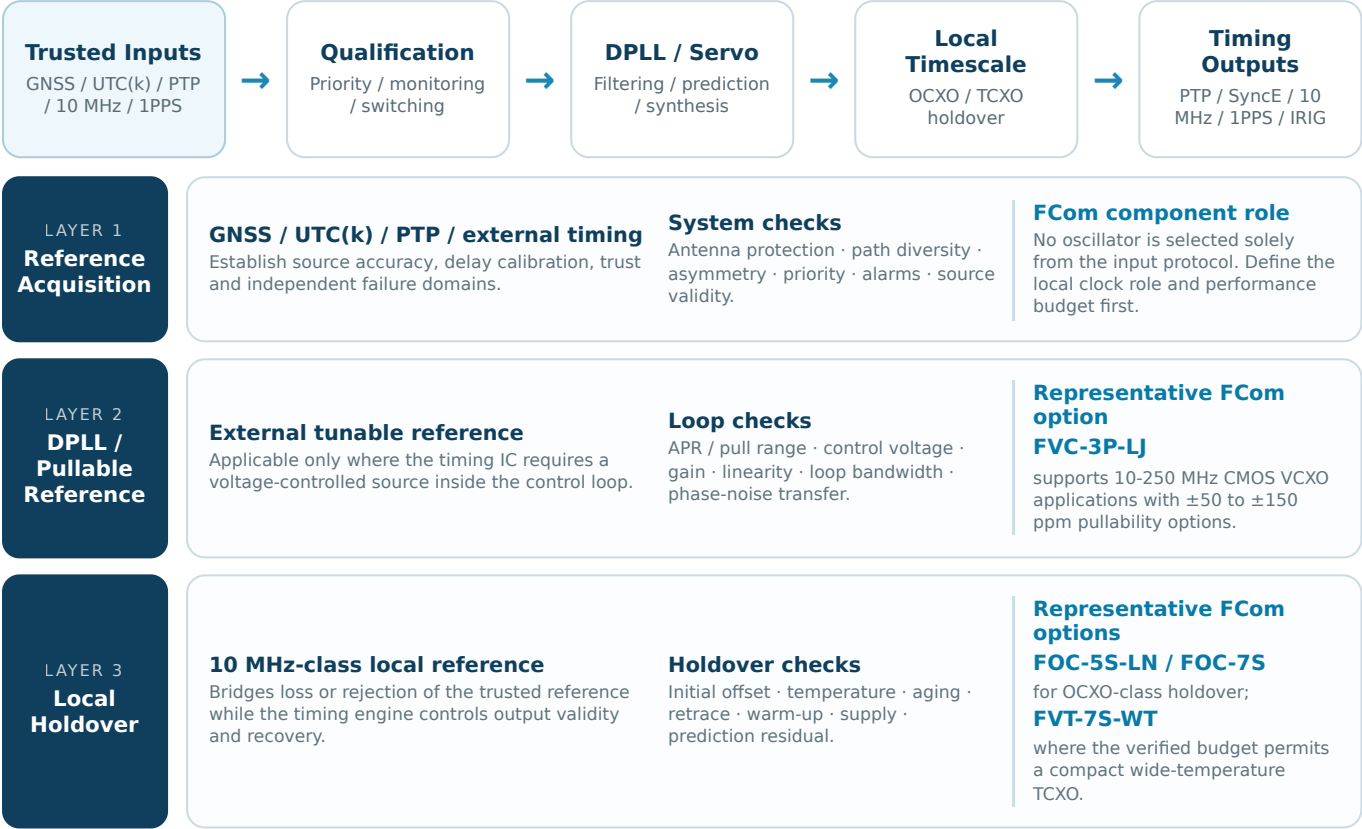
Selection insight: multi-format time servers typically require both a qualified holdover oscillator and independent board / data clocks.

Platform interpretation: these public examples illustrate representative architectures only. They do not indicate FCom adoption, qualification, verified compatibility or drop-in replacement. Final selection is based on the target-device documentation, schematic and complete timing requirements.

05

Protected Reference + Local Holdover Architecture

Representative timing path from trusted-reference acquisition through qualification, steering, holdover and controlled output distribution.

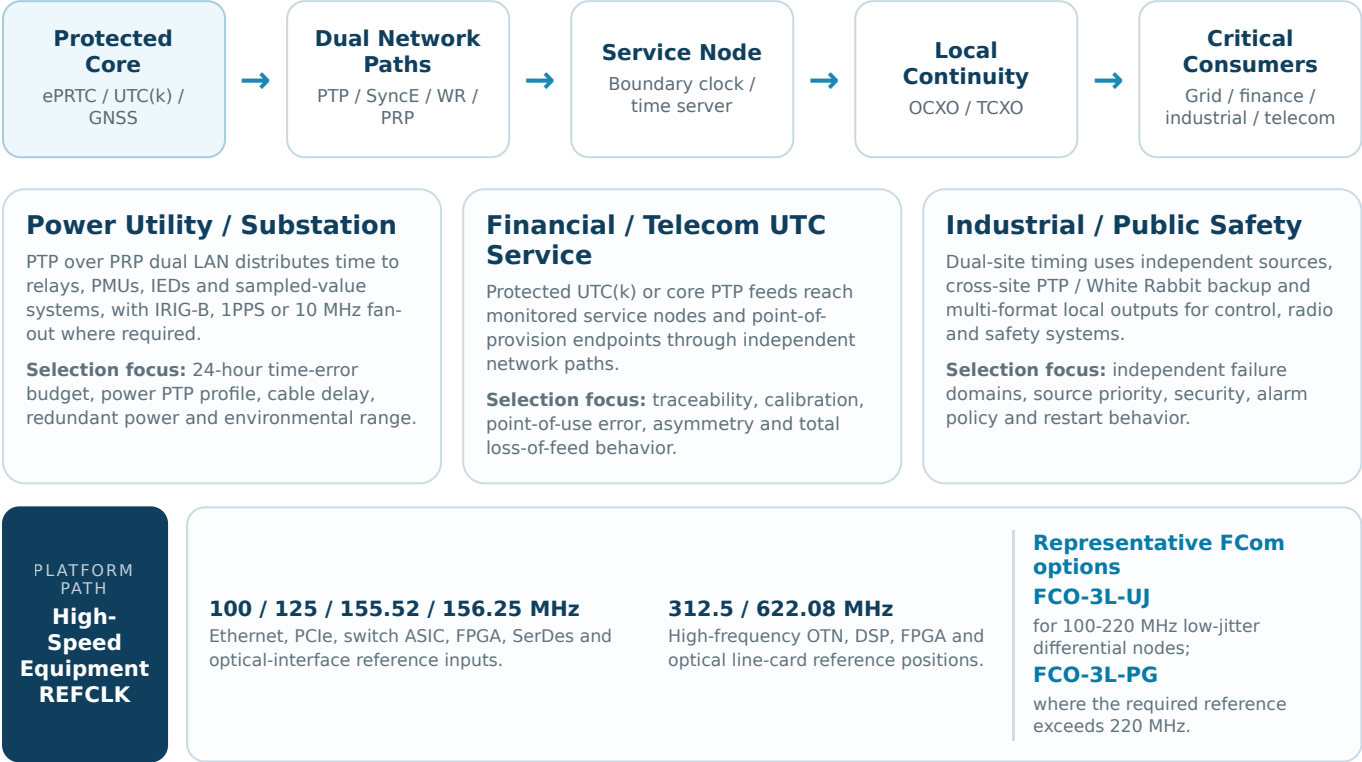


Holdover calculation note: a constant 10 ppb frequency error contributes approximately 0.864 ms of time error in 24 hours; 50 ppb contributes approximately 4.32 ms. These are illustrative calculations, not guaranteed holdover performance for any product.

06

Resilient Distribution + Endpoint Clocking Architecture

Representative timing from protected core references through redundant networks into critical service nodes and high-speed equipment clock domains.



07

FCom Selection Guidance by Design Condition

The product families below correspond to four clock decisions where holdover, temperature, pullability or jitter materially changes component selection.

Extended Holdover

10 MHz-class low-aging OCXO for protected local timescale continuity.

Compact Precision

High-stability TCXO where the validated holdover budget permits a smaller footprint and lower power consumption.

Pullable DPLL Reference

VCXO only where the timing IC requires external voltage control.

Low-Jitter REFCLK

Differential high-speed reference selected by device mask and frequency.

Design Condition	FCom Selection	Why It Changes the Decision	Key Check Before RFQ
10 MHz-class holdover with low aging / phase noise	FOC-5S-LN / FOC-7S	FOC-5S-LN emphasizes close-in phase noise in a 14 x 9 mm package; FOC-7S provides a compact 9 x 7 mm OCXO path. Both families support 10-40 MHz, with ± 5 ppb frequency-stability options.	time-error budget · aging · phase-noise mask · package · supply
Compact timing node with operation to +105°C	FVT-7S-WT	7050 high-stability TCXO covering 10-52 MHz, 2.5 / 3.3 V, clipped sine or CMOS, with ± 50 ppb and -40 to +105°C options.	outage duration · output · power · temperature · 10 MHz phase noise
DPLL explicitly requires an external tunable CMOS reference	FVC-3P-LJ	3225 CMOS VCXO covering 10-250 MHz with ± 50 to ± 150 ppm pullability options for defined recovery-loop architectures.	APR · control voltage · gain · linearity · loop bandwidth · VDD
Differential high-speed REFCLK with explicit jitter mask	FCO-3L-UJ / FCO-3L-PG	FCO-3L-UJ covers 100-220 MHz with LVPECL / LVDS / HCSL output options and 50 fs-class RMS jitter performance; FCO-3L-PG extends LVPECL / LVDS frequency coverage up to 1500 MHz.	frequency · output logic · jitter band · termination · VDD

Application-specific extensions: passive 32.768 kHz crystals are relevant only where the RTC / controller exposes an external resonator input. Crystal Filter and SAW products address separate RF / IF filtering functions and sit outside the primary timing and holdover chain. Exact series configuration and ordering code are confirmed during FCom application review.

ENGINEERING SELECTION SUPPORT

Request an FCom Critical-Network Timing Recommendation

Provide the clock-tree diagram, target timing IC / processor / PHY, node role, frequency, time-error or jitter budget, output interface, operating temperature and project stage.

[Start Engineering Review →](#)

08 Engineering Validation & Minimum RFQ

Critical-network timing is defined by clock role, outage-time error, servo architecture and receiving interface in addition to frequency.

Trusted Source & Holdover

- Source hierarchy and independence
- Maximum outage duration
- Permitted phase / time error
- Aging, retrace and warm-up
- Temperature profile
- Calibration interval

DPLL & Network Sync

- Exact timing IC / module P/N
- PTP / SyncE / GNSS / 1PPS topology
- Fixed or pullable local reference
- Loop bandwidth / APR
- Switching and recovery behavior
- Wander and phase continuity

Platform REFCLK

- Target processor / PHY / FPGA P/N
- Frequency and source direction
- CMOS / LVDS / LVPECL / HCSL
- RMS jitter and integration band
- Termination and load
- SSC / OE requirements

Environment & Program

- Operating temperature and airflow
- Supply-noise environment
- Package / height
- Qualification and compliance
- Prototype / production schedule
- Estimated annual usage

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	ePRTC / PRTC, grandmaster, SSU / BITS, substation clock, UTC service node, time server, DPLL reference, platform REFCLK or RTC.
Target Device	Exact receiving IC / module part number, clock pin, schematic location and block diagram.
Timing Objective	Maximum phase / time error, outage duration, recovery limit, traceability objective and calibration interval.
Oscillator Requirements	Frequency, stability, aging, retrace, warm-up, phase-noise mask, RMS jitter / integration band and pull range if required.
Electrical / Mechanical	VDD, output logic, load, termination, OE / standby, package, height and operating temperature.
Program Requirements	Prototype quantity, sample date, validation plan, annual volume, production location, lifecycle and compliance documentation.

10 MHz Does Not Define Holdover

The result depends on oscillator grade, initial offset, temperature, aging, retrace and disciplining history.

1PPS Does Not Replace the Local Oscillator

The timing engine still requires a local source to interpolate between pulses and continue through an outage.

156.25 MHz Is a Platform REFCLK

A low-jitter SerDes clock and a high-stability holdover oscillator serve different consumers and use different metrics.

Frequency alone does not define the final part: the clock role, receiving device, time-error or jitter budget, interface and environmental profile determine the appropriate FCom series and exact electrical configuration.

09

Engineering FAQ & Application Review

Common critical-network timing questions, representative public references and the information required for FCom engineering review.

Does a 10 MHz output prove long holdover?

No. Frequency alone does not define holdover. Oscillator grade, initial offset, temperature, aging, retrace and disciplining history determine the result.

When should an OCXO replace a TCXO?

When calculated outage-time error, aging, phase-noise or environmental requirements exceed the verified TCXO capability.

Can a 156.25 MHz data clock replace the holdover reference?

No. A low-jitter SerDes reference and a high-stability holdover oscillator serve different nodes and are specified with different metrics.

Can a timing system operate from 1PPS without a local oscillator?

A 1PPS input establishes phase / time alignment, but the timing engine requires a local oscillator to interpolate between pulses and continue during an outage.

What makes the oscillator important in a PTP system?

It affects servo noise, packet-delay filtering, phase continuity and holdover. Network asymmetry and timestamping architecture remain equally important.

Does the protocol determine the oscillator?

No. PTP, NTP, SyncE and White Rabbit define system transport. The local oscillator follows the servo, outage and receiving-interface requirements.

When is a VCXO required?

Only when the timing IC explicitly requires an external voltage-controlled reference with a defined APR, control range and loop architecture.

Are SAW or crystal filters part of every timing BOM?

No. They apply only to defined RF or IF signal paths and are not standard elements of the primary timing and holdover chain.

Representative Public Technical References

1. **Microchip:** TimeProvider 4100 - PTP / NTP / SyncE, vPRTC / ePRTC and legacy timing architecture.
2. **Microchip:** TimeCesium PRS - cesium reference and ePRTC configuration.
3. **SEL:** SEL-2488 specifications - PTP / PRP, IRIG-B / 1PPS / 10 MHz and oscillator-dependent holdover.
4. **NPL:** NPLTime FAQ and UBS case material - UTC(NPL), dual-fiber PTP and local cesium holdover.
5. **Safran:** SecureSync 2400 and WROX - modular timing I/O and dual-site White Rabbit / PTP architecture.
6. **Safran:** SecureSync holdover mode - oscillator-dependent drift and output behavior during reference loss.
7. **Microchip:** ZL30132 - representative telecom, Ethernet and high-speed reference frequencies.

FCom product specification note: product information in this guide is presented at series or representative-configuration level. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

Timing Infrastructure & Critical Networks Review

Provide the system architecture, clock node, target timing IC / processor / PHY, frequency, time-error or jitter target, output interface, operating temperature, package and project stage. FCom application engineering can review the requirement and recommend a suitable series and configuration for system-level validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.