

## PACKET TRANSPORT &amp; NETWORK TIMING

# Switching, Routing & Mobile Transport

Timing and frequency-control solutions for packet transport and telecom networking platforms requiring synchronized timing, high-speed PHY / SerDes clocking and clock recovery.

**Network Synchronization + PHY / SerDes Clocking + Clock Recovery**

Core / Edge Routers

Carrier Ethernet

Cell-Site Routers

Fronthaul / Backhaul

Timing Cards

Microwave Transport

**Application Scope**

Carrier-grade switching, routing and mobile-transport platforms combining network synchronization, packet processing, high-speed Ethernet / SerDes and recovered-clock domains.

**Relevant FCom Device Families**

**Primary:** OCXO · TCXO · VCXO · Low-Jitter Differential XO · Differential XO · CMOS XO · Quartz Crystal

**Architecture-dependent:** SAW Filter · MCF Crystal Filter · SAW Resonator

**Sync**

IEEE 1588 PTP, SyncE, GNSS / external references and holdover.

**Packet**

Switch ASIC, FPGA, processor and line-card reference clocks.

**SerDes**

Low-jitter PHY / SerDes reference clocking for high-speed Ethernet.

**Recovery**

Recovered-clock, DPLL and jitter-attenuation architectures.

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# Application Scope & System Architecture

**Switching, Routing & Mobile Transport** covers packet-transport and telecom-networking platforms requiring synchronized network timing, stable local clocking, low-jitter high-speed references and architecture-specific clock recovery.

## Representative Equipment

### Routing & Aggregation

- Core / Edge Routers
- Aggregation / Carrier Ethernet Switches
- Telecom Line Cards
- Telecom Gateways

### Mobile Transport

- Cell-Site Routers
- Fronthaul / Backhaul Switches
- Timing / Synchronization Cards
- Mobile Transport Gateways

### Wireless Backhaul

- Microwave Backhaul Equipment
- Packet / Radio Aggregation Nodes
- Outdoor / Hardened Transport
- Mixed Fiber / Microwave Transport

## Four Engineering Domains

### Network Synchronization

PTP · SyncE · GNSS / 10 MHz / 1PPS · timing hierarchy · holdover · aging.

### Packet / ASIC Clocking

Switch ASIC · FPGA · processor · line-card logic · management clock domains.

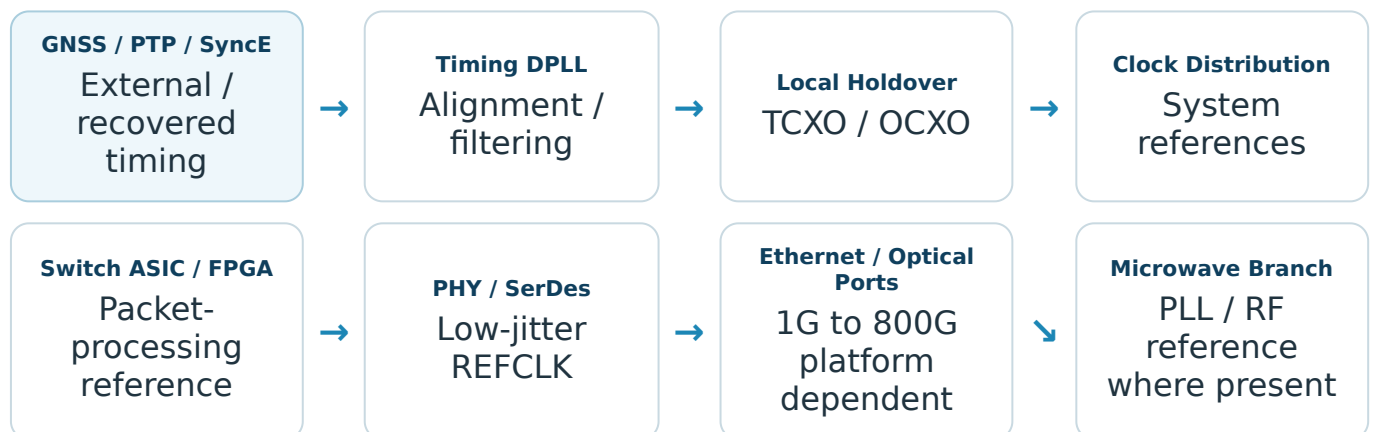
### PHY / SerDes & Recovery

Ethernet PHY · SerDes REFCLK · recovered clock · DPLL / jitter attenuation.

### Mobile Transport Radio

Microwave modem / radio reference · RF synthesizer clock · selected RF / IF filtering.

## Representative End-to-End Clock Path



**Architecture rule:** line rate and internal processing clock do not automatically define an external oscillator frequency. Confirm the actual DPLL, switch ASIC, FPGA, PHY or SerDes reference-clock input first.

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## Select by System Node First

Begin with the target clock node and its function. Confirm whether the reference is externally supplied, recovered from the network or generated internally, then select the appropriate device class and performance level.

| System Node                            | Typical Function                         | Representative Frequency                          | Preferred Device Class                  | Selection Focus                                                                                     |
|----------------------------------------|------------------------------------------|---------------------------------------------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------|
| Timing / Holdover Module               | PTP / SyncE timing continuity            | <b>10 / 20 / 30.72 / 38.88 MHz</b>                | OCXO / High-Stability TCXO              | ppb stability, aging, holdover, temperature                                                         |
| Timing DPLL Reference                  | Local reference for synchronization loop | <b>19.2 / 19.44 / 20 / 25 / 30.72 / 38.88 MHz</b> | TCXO / OCXO                             | Stability, phase noise, temperature, aging                                                          |
| External Tunable / Jitter-Cleaner Node | PLL control / recovered-clock tracking   | <b>122.88 / 125 / 156.25 MHz*</b>                 | VCXO                                    | Confirm whether an external VCXO is required; then define APR / pull range and electrical interface |
| Ethernet PHY / Local Reference         | PHY or management clock                  | <b>25 / 50 / 62.5 MHz</b>                         | Quartz Crystal / CMOS XO                | CL / ESR or supply / logic / startup                                                                |
| Switch ASIC / FPGA                     | Packet / fabric / PLL reference          | <b>100 / 125 MHz</b>                              | CMOS / Differential XO                  | Jitter, output logic, signal integrity                                                              |
| High-Speed SerDes                      | 10G+ Ethernet / transceiver REFCLK       | <b>125 / 156.25 MHz</b>                           | Low-Jitter Differential XO              | Integrated RMS jitter, differential logic, termination                                              |
| Advanced SerDes / Clock Synthesis      | Platform-specific external REFCLK        | <b>312.5 MHz+</b>                                 | High-Frequency Differential XO          | Confirm the external requirement and full jitter budget                                             |
| Management / RTC                       | Housekeeping / timekeeping               | <b>25 / 50 MHz + 32.768 kHz</b>                   | Crystal / CMOS XO / Tuning-Fork Crystal | Power, startup, package, temperature                                                                |

### Synchronization Node

Prioritize long-term stability, aging, holdover and temperature before package size.

### SerDes Node

Prioritize RMS jitter, LVDS / LVPECL / HCSL compatibility, termination and routing.

### Recovered-Clock Node

Use an external VCXO only where the selected DPLL or jitter-cleaner architecture requires a tunable reference.

**Selection guidance:** frequency alone does not define the correct component. Final selection should also consider the system node, output interface, stability or jitter target, operating temperature and package constraints.

# 03 Frequency & Component Placement Matrix

Evaluate each frequency together with its system position and clock role. Product selection follows after the external reference requirement, interface type and performance budget have been confirmed.

| Frequency / Family                         | Typical System Position                         | Reference Status       | Preferred Device Class         | Engineering Interpretation                                                                                              |
|--------------------------------------------|-------------------------------------------------|------------------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------|
| 10 MHz                                     | Master reference / holdover / timing card       | Common External        | OCXO                           | Precision synchronization anchor; holdover and aging dominate                                                           |
| 19.2 / 19.44 / 20 / 25 / 30.72 / 38.88 MHz | PTP / SyncE DPPL reference                      | Common External        | TCXO / OCXO                    | Telecom timing family; select stability class from the holdover budget                                                  |
| 25 / 50 / 62.5 MHz                         | PHY / local clock / timing IC                   | Common External        | Crystal / CMOS XO              | Typically selected according to startup margin, electrical interface, package and cost rather than holdover performance |
| 77.76 / 100 / 125 MHz                      | Legacy transport / FPGA / switch logic          | Platform-Dependent     | CMOS / Differential XO         | Confirm whether the target IC expects single-ended or differential input                                                |
| 122.88 / 125 / 156.25 MHz                  | External tunable PLL / recovered-clock node     | Architecture-Dependent | VCXO                           | Use only when an external tunable reference is documented                                                               |
| 125 / 156.25 MHz                           | Ethernet / ASIC / FPGA / SerDes                 | Common External        | Low-Jitter Differential XO     | Primary high-speed clocking range for this application                                                                  |
| 155.52 MHz                                 | Mixed-generation SONET / SDH transport          | Legacy / Mixed Network | Differential XO                | Retain where transport equipment must bridge legacy timing domains                                                      |
| 312.5 MHz+                                 | Selected high-speed SerDes / synthesizer REFCLK | Platform-Dependent     | High-Frequency Differential XO | Confirm whether the selected transceiver requires this frequency as an external board-level reference                   |

## Ethernet Clock Family

25 / 50 / 62.5 / 125 / 156.25 / 312.5 MHz appear across Ethernet timing and transport architectures, but not every value is an external oscillator node.

## Telecom Timing Family

19.44 / 38.88 / 77.76 / 155.52 MHz remain relevant in mixed-generation transport and synchronization environments.

## External vs Derived

Internal ASIC, FPGA and transceiver clocks can be much higher than the board reference. Select an oscillator only for a documented external REFCLK.

**Selection note:** representative FCom series are introduced in the following sections where their specifications help clarify device selection for specific clock nodes.

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## Representative Platform & Architecture Matrix

The following public platforms illustrate representative synchronization, packet-processing and high-speed interface architectures. FCom solutions are referenced by functional suitability only and do not imply original-platform adoption, qualification or pin-to-pin compatibility.

### CISCO

#### NCS 540 Large Density Router

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**Platform overview:** carrier routing platform with SyncE, IEEE 1588 PTP, integrated GNSS and 10 MHz / 1PPS / ToD timing interfaces; high-speed Ethernet configurations extend to 400GE.

**Clock architecture:** precision synchronization and packet / SerDes clocking are separate domains.

GNSS / 10 MHz / PTP / SyncE → Timing / Holdover → ASIC / PHY / SerDes

**FCom application direction:** evaluate a precision timing class for holdover and a separate low-jitter differential clock class for high-speed REFCLK nodes.

### JUNIPER

#### ACX7024 / ACX7024X Cloud Metro

2

**Platform overview:** GNSS-backed Assisted Partial Timing Support (APTS); GNSS is the preferred source, G.8275.2 packet timing can back it up, and the internal clock supports a holdover-in-spec state.

**Clock architecture:** the platform illustrates a three-level timing hierarchy: GNSS → packet timing backup → local holdover.

GNSS → PTP Backup → Local Holdover

**FCom application direction:** first determine the required holdover class, then choose TCXO or OCXO; package is a secondary decision.

### NOKIA

#### 7250 IXR-X1b / X3b / X4

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**Platform overview:** up to 25.6 Tb/s in 1RU, interfaces through 800GE, with SyncE and IEEE 1588v2 capabilities.

**Clock architecture:** high line rate raises the importance of low-jitter ASIC / SerDes reference clocking, but does not define the external oscillator frequency by itself.

SyncE / PTP Domain + Switch ASIC / SerDes → 100G / 400G / 800G

**FCom application direction:** select the differential clock only after the exact ASIC / SerDes REFCLK frequency, output logic and RMS-jitter mask are known.

### ERICSSON

#### MINI-LINK 6600 Mobile Transport

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**Platform overview:** packet aggregation with 1 / 10 / 25GE interfaces; Ericsson documents PTP G.8275.1 support with Class B performance or better and SyncE over microwave radio hops.

**Clock architecture:** packet synchronization and the microwave modem / RF synthesizer domain must be evaluated separately.

PTP / SyncE → Packet / Ethernet → Microwave Modem / RF

**FCom application direction:** timing products apply to the packet-sync domain; RF / IF filtering is architecture-dependent and must remain within the actual FCom filter-frequency range.

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# Packet Transport Timing & Clock Architecture

This representative architecture separates synchronization and holdover, tunable clock recovery, packet-processing clocks and high-speed SerDes references. Representative FCom series are shown only at nodes where their specifications support a clear engineering selection.

|                                                      |                                                      |                                                                                                     |                                                                                                                                                                                                                                                                                                                                       |
|------------------------------------------------------|------------------------------------------------------|-----------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>LAYER 1</b><br><b>External Timing</b>             | <b>GNSS / BITS</b><br>Absolute / frequency reference | <b>PTP → SyncE</b><br>Packet phase / time · Physical-layer frequency                                | <b>Timing source definition</b><br>Define the timing hierarchy, source priority and required holdover interval before selecting the local reference.                                                                                                                                                                                  |
| <b>LAYER 2</b><br><b>Timing &amp; Holdover</b>       | <b>Timing Receiver</b><br>PTP / SyncE recovery       | <b>Timing DPLL → Local Holdover</b><br>Frequency / phase alignment · Continuity during source loss  | <b>Selection anchor: FOC-5S-LN or FVT-7S-WT</b><br>Use OCXO when holdover / ppb stability dominates; use the $\pm 50$ ppb TCXO class when lower power and wide temperature are sufficient.<br>FOC-5S-LN: 10–40 MHz · $\pm 5$ ppb · $-40 \sim +85^\circ\text{C}$   FVT-7S-WT: 10–52 MHz · $\pm 50$ ppb · $-40 \sim +105^\circ\text{C}$ |
| <b>LAYER 3</b><br><b>Clock Recovery / Cleaning</b>   | <b>Recovered Clock</b><br>Line / network derived     | <b>DPLL / Jitter Cleaner → Clean Reference</b><br>Tracking and cleanup · Redistribution             | <b>Conditional anchor: FVC-3P-LJ</b><br>Only where the selected DPLL documents an external CMOS VCXO.<br>10–250 MHz · 2.5 / 3.3 V · pull $\pm 50$ to $\pm 150$ ppm · $-40 \sim +105^\circ\text{C}$                                                                                                                                    |
| <b>LAYER 4</b><br><b>Packet Processing</b>           | <b>Switch ASIC</b><br>Packet forwarding / fabric     | <b>FPGA → Management SoC</b><br>Protocol / acceleration · Control plane                             | <b>Local clock selection</b><br>Select a Quartz Crystal, CMOS XO or Differential XO according to the receiving clock input, electrical interface and jitter requirement.                                                                                                                                                              |
| <b>LAYER 5</b><br><b>PHY / SerDes</b>                | <b>PHY / MAC</b><br>Ethernet interface               | <b>SerDes → Optical / Line Port</b><br>High-speed transceiver · Transport interface                 | <b>Selection anchor: FCO-2L-UJ / FCO-3L-UJ</b><br>Use for 125 / 156.25 MHz-class low-jitter differential REFCLK nodes when the target interface requires it.<br>100–220 MHz · LVPECL / LVDS / HCSL · $\pm 20$ ppm · $-40 \sim +125^\circ\text{C}$ · 50 fs                                                                             |
| <b>LAYER 6</b><br><b>Advanced / Microwave Branch</b> | <b>High-Frequency REFCLK</b><br>Platform-specific    | <b>RF Synthesizer → RF / IF Filter Path</b><br>Microwave / radio reference · Architecture dependent | <b>Conditional anchor: FCO-3L-PG</b><br>Use only when a higher external differential REFCLK such as 312.5 MHz is explicitly required and its jitter meets the receiving budget. RF / IF filters remain mask-driven.<br>10–1500 MHz · LVPECL / LVDS · 0.6 ps catalog jitter · $-40 \sim +105^\circ\text{C}$                            |

**Reference-design note:** the component type should follow the clock function at each node. Representative FCom series are shown only where their performance class materially affects system selection.

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## Device Selection by System Function

Select the device architecture according to the clock function and performance requirement. A representative FCom series is provided where its specification helps define the appropriate solution class.

### OCXO

**Recommended when:** holdover, aging and ppb-class stability dominate.

Key inputs: holdover interval, aging, warm-up, close-in phase noise, size and power.

### High-Stability TCXO

**Recommended when:** compact size and lower power are preferred and  $\pm 50$  ppb-class stability meets the timing budget.

Key inputs: temperature range, stability, output format and phase noise.

### VCXO

**Recommended when:** the DPLL / PLL explicitly requires an external tunable reference.

Key inputs: APR / pullability, control voltage, output interface and frequency range.

### Low-Jitter Differential XO

**Recommended when:** ASIC / FPGA / PHY / SerDes jitter budget is the primary constraint.

Key inputs: RMS jitter, LVDS / LVPECL / HCSL, supply, termination and temperature.

### Crystal / CMOS XO

**Recommended when:** the node is a local PHY, processor or management reference without precision synchronization requirements.

Key inputs: CL / ESR or supply / logic, startup, package and power.

### RF / IF Filter

**Applicable when:** the actual mobile-transport architecture includes a supported lower-frequency RF / IF or narrowband IF filter node.

Selection requires the complete mask; never select from center frequency alone.

## Representative FCom Selection Examples

| Decision Point                  | Representative FCom Series           | Selection Rationale                                                                                                                        | Final Parameters to Confirm                          |
|---------------------------------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|
| OCXO vs TCXO holdover           | <b>FOC-5S-LN</b> vs <b>FVT-7S-WT</b> | Illustrates the tradeoff between tighter OCXO stability and a compact wide-temperature TCXO solution.                                      | Holdover budget, aging, warm-up, power               |
| External tunable clock          | <b>FVC-3P-LJ</b>                     | Provides a 10-250 MHz CMOS VCXO option with $\pm 50$ to $\pm 150$ ppm pullability for tunable-reference applications.                      | DPLL external-VCXO requirement, APR, control voltage |
| 125 / 156.25 MHz SerDes REFCLK  | <b>FCO-2L-UJ</b> / <b>FCO-3L-UJ</b>  | Provides a 100-220 MHz ultra-low-jitter differential range with LVPECL, LVDS and HCSL output options.                                      | Jitter mask, output logic, supply, termination       |
| 312.5 MHz-class external REFCLK | <b>FCO-3L-PG</b>                     | Provides higher-frequency differential coverage above 220 MHz for applications whose jitter budget allows the specified performance class. | External REFCLK need and whether 0.6 ps meets budget |

**Additional local-clock options:** FCom Quartz Crystal, CMOS XO and 32.768 kHz families are available for PHY, management and RTC nodes. The exact series should be selected after package, CL / ESR, supply-voltage and output requirements are defined.

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## Representative FCom Solutions by Selection Need

The following representative FCom series cover key timing, synchronization and high-speed reference-clock requirements found in switching, routing and mobile-transport platforms.

| Selection Need                            | Representative Series        | Representative Specifications                                                                               | Use When                                                                           | Selection Boundary                                                                           |
|-------------------------------------------|------------------------------|-------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|
| <b>Precision Holdover</b>                 | <b>FOC-5S-LN</b>             | 10-40 MHz · 14×9 6-SMD · 3.3 / 5 V · ±5 ppb · -40~+85°C · rectangular · PN -162 dBc/Hz @10 kHz              | Holdover / low-noise master reference where ppb stability is justified             | Apply only where the system holdover and stability requirements justify an OCXO              |
| <b>Wide-Temperature Telecom Timing</b>    | <b>FVT-7S-WT</b>             | 10-52 MHz · 7050 4-SMD · 2.5 / 3.3 V · ±50 ppb · -40~+105°C · clipped sine / CMOS · VCTCXO pull ±5 ppm      | TCXO-class synchronization where size, power and +105°C matter                     | Confirm that the required holdover and aging performance can be achieved with the TCXO class |
| <b>External Tunable DPLL Reference</b>    | <b>FVC-3P-LJ</b>             | 10-250 MHz · 3225 6-SMD · 2.5 / 3.3 V · CMOS · stability ±25 to ±50 ppm · pull ±50 to ±150 ppm · -40~+105°C | The selected PLL / jitter cleaner explicitly requires an external VCXO             | Use only where the selected DPLL / PLL requires an external tunable reference                |
| <b>125 / 156.25 MHz Low-Jitter REFCLK</b> | <b>FCO-2L-UJ / FCO-3L-UJ</b> | 100-220 MHz · 2520 / 3225 6-SMD · 1.8 / 2.5 / 3.3 V · ±20 ppm · -40~+125°C · LVPECL / LVDS / HCSL · 50 fs   | ASIC / FPGA / PHY / SerDes reference inputs with a stringent jitter budget         | Match output logic, termination, supply and the receiver jitter mask before release          |
| <b>High-Frequency External REFCLK</b>     | <b>FCO-3L-PG</b>             | 10-1500 MHz · 3225 6-SMD · 2.5 / 3.3 V · ±25 ppm · -40~+105°C · LVPECL / LVDS · 0.6 ps                      | 312.5 MHz+ external differential references when required and within jitter budget | Do not apply the 50 fs UJ specification above the UJ series frequency range                  |

### Local PHY / Management Clocks

FCom Quartz Crystal and CMOS XO families support local PHY, processor and management-clock nodes. Select the exact series from the receiving input, frequency, package and electrical requirements.

### RTC / Housekeeping

FCom 32.768 kHz tuning-fork crystals are available for RTC and low-power timekeeping functions where required by the platform.

### RF / IF Filters

SAW and MCF solutions are architecture-dependent. A specific filter can be selected after the RF / IF center frequency, bandwidth, insertion loss and rejection mask are defined.

#### SELECTION SUPPORT

### Request an Exact FCom Ordering Recommendation

Provide the target IC or module, clock-node function, frequency, supply voltage, output logic, stability / jitter / phase-noise target, operating temperature and package constraints. FCom can then recommend the appropriate series and confirm the frequency-specific ordering code.

[Prepare RFQ Inputs →](#)

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## Engineering Validation & Selection Checklist

For design-in and production release, confirm the complete timing hierarchy, clock interface and performance requirements before finalizing the FCom ordering code.

### Synchronization / Holdover

- GNSS / PTP / SyncE hierarchy and reference priority
- 10 MHz / 1PPS / ToD / BITS interface requirement where applicable
- Frequency / phase holdover duration and allowed drift
- Temperature stability, aging, warm-up, MTIE / TDEV requirements

### PHY / SerDes / ASIC

- Exact REFCLK pin and external-reference requirement
- Frequency, LVDS / LVPECL / HCSL / CMOS logic
- RMS jitter integration bandwidth and receiver mask
- Termination, swing, rise/fall time, fan-out and routing

### VCXO / Clock Recovery

- Confirm external VCXO is required by the selected DPLL
- APR / pull range and control-voltage range
- Nominal frequency and output logic
- Phase-noise / spur requirements at specified offsets

### Quartz / Local Clock

- Frequency, CL, ESR, C0 and drive level
- Negative resistance / startup margin on final PCB
- Initial tolerance and temperature stability
- Supply / current / package when using active CMOS XO

## Minimum RFQ Information

| Information Category   | What to Provide                                                                                                                             |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Platform / System Node | Router / switch / line card / timing card / cell-site router / microwave node; exact target IC, module and clock pin.                       |
| Clock Role             | Master reference, holdover, DPLL local reference, recovered-clock support, ASIC / PHY / SerDes REFCLK, management clock or RF reference.    |
| Oscillator             | Frequency, voltage, output, stability, temperature, jitter / phase noise, package, OE, pullability and warm-up / aging where applicable.    |
| Quartz Crystal         | Frequency, CL, ESR, C0, drive level, tolerance, stability, temperature and package.                                                         |
| SAW / MCF              | Center frequency, passband, insertion loss, ripple, full rejection mask, impedance / VSWR, package, temperature and RF power.               |
| Project / Program      | Prototype quantity, required sample date, qualification stage, annual volume, production site and environmental / reliability requirements. |

### Line Rate $\neq$ Reference Frequency

100G / 400G / 800G interface speed does not by itself define the required board-level reference-clock frequency.

### Frequency Alone Is Insufficient

A 156.25 MHz requirement must also define output logic, jitter budget, supply voltage, package and operating temperature.

### Filter Frequency Range

FCom SAW solutions should be applied only within the supported frequency range and with a complete RF mask. Higher microwave-carrier filtering requires a different RF solution.

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## Engineering FAQ & Application Review

### Is 156.25 MHz always the correct Ethernet oscillator?

No. It is a common high-speed Ethernet / SerDes reference family, but the actual external REFCLK must follow the selected ASIC, PHY or FPGA transceiver documentation.

### How should a 312.5 MHz external reference be evaluated?

The FCO-2L-UJ / FCO-3L-UJ ultra-low-jitter range extends to 220 MHz. For a 312.5 MHz external reference, use a higher-frequency differential series and verify that its specified jitter meets the receiving interface budget.

### When is OCXO preferred over TCXO?

Use OCXO when holdover, tighter ppb stability, aging or close-in phase noise dominate. Use TCXO when the required stability can be achieved with smaller size and lower power.

### Does clock recovery always need an external VCXO?

No. Some modern network DPLLs integrate NCO / synthesizer functions. Use an external VCXO only when the selected timing architecture requires one.

### Are FCom SAW filters intended for 11 / 13 GHz microwave carrier filtering?

The FCom SAW portfolio represented in this guide extends to approximately 3.55 GHz. Direct filtering at 11 / 13 GHz therefore requires a different RF technology and is outside the scope of the SAW solutions presented here.

### Where do SAW / MCF products fit?

They apply to selected lower-frequency RF / IF or narrowband IF signal paths. Their use depends on the actual mobile-transport radio or receiver architecture and should be specified from the complete filter mask.

## Primary Public Technical References

1. **Cisco:** NCS 540 Large Density Router — SyncE, PTP, integrated GNSS and high-speed Ethernet platform context.
2. **Cisco:** NCS 540 timing interfaces — 10 MHz, 1PPS, ToD and GNSS hardware interfaces.
3. **Juniper:** ACX7024 APTS — GNSS primary, G.8275.2 backup and internal holdover state.
4. **Nokia:** 7250 IXR family — high-speed interface and SyncE / IEEE 1588v2 platform context.
5. **Ericsson:** MINI-LINK 6600 — packet aggregation and mobile-transport context.
6. **Microchip:** DS3102 — representative Ethernet / SONET / SDH timing frequency families.

### ENGINEERING REVIEW

## Switching, Routing & Mobile Transport Application Review

Share the platform type, target IC / module, exact clock node, required frequency, output logic, stability / jitter / phase-noise target, temperature, package and project stage. FCom can then recommend the appropriate product series and confirm the frequency-specific ordering code.

[Request Engineering Review →](#)
[Technical Support](#)

This guide provides representative application and selection guidance. Public platform references illustrate clock-domain architecture only. Final selection must be verified against the latest target-device documentation and the exact FCom product specification, then validated on the complete board and system.