

SMARTPHONES & TABLETS

Smartphones & Tablets Timing Solutions

This guide supports selection of the physical reference sources used for application processing, wireless connectivity, always-on RTC, GNSS and multimedia / peripheral clock domains across battery-powered mobile platforms.

SoC Main Clock + Wireless Reference + RTC Low Power + GNSS Stability + Camera / Display / Peripheral Timing

Smartphones

Tablets & 2-in-1

Wireless Connectivity

GNSS

RTC / Always-On

Camera / Display / I/O

Application Scope

Smartphones, tablets, rugged handhelds, mobile POS terminals, connected modules and consumer platforms using discrete or externally driven timing references.

Selection Philosophy

Selection begins with the receiving clock node. A passive crystal, CMOS oscillator, clipped-sine TCXO and 32.768 kHz source are different electrical classes even when their nominal frequencies appear in the same platform.

SoC / Baseband

Application-processor and baseband PLL reference.

Wireless / GNSS

Cellular, Wi-Fi, Bluetooth, RF and positioning timing.

RTC / Always-On

Sleep, retained-time and low-power wake domain.

Multimedia / I/O

Camera, display, touch, USB and bridge references.

01

Application Scope & Engineering Domains

Mobile platforms combine active, sleep, RF and multimedia clock domains; only some of those domains expose a replaceable physical reference source.

One platform, multiple timing domains. The SoC, wireless device, GNSS chain, PMIC / RTC and peripheral bridges may use independent sources, share a reference or receive a clock generated elsewhere on the board.

Typical Equipment

Handsets & Tablets

Mainstream smartphone
Consumer tablet
Education tablet
2-in-1 platform
Rugged handheld

Enterprise & Embedded Mobile

Mobile POS terminal
Enterprise handheld
Industrial tablet
Cellular gateway
Embedded consumer platform

Connected Subsystems

Wi-Fi / Bluetooth module
GNSS subsystem
Camera / display module
USB-C dock
High-speed bridge

Four Engineering Domains

SoC & Baseband

19.2 / 24 / 26 / 38.4 MHz-class processor and PLL reference.

Wireless & GNSS

24 / 26 / 38.4 / 40 MHz radio or stable positioning reference.

RTC & Always-On

32.768 kHz crystal loop or low-current external CLKIN.

Multimedia & I/O

Camera MCLK, display bridge, USB and high-speed REFCLK.

Clock Interface

XTAL pins · CMOS CLKIN · clipped-sine TCXO input · differential REFCLK.

Low-Power State

Separate always-on / backup timing from active AP, RF and multimedia clocks.

RF Performance

Evaluate total error, phase noise, harmonics, drive level and physical placement.

Generated Clocks

CPU GHz, MIPI lane rate, pixel clock and interface data rate are normally synthesized or forwarded.

Clock-definition note: application-processor operating frequency, display refresh rate, camera frame rate, cellular band, GNSS update rate and interface data rate do not directly define the external crystal or oscillator frequency.

02

Select by System Node First

Begin with the receiving clock input, then determine frequency, device class, performance requirements and package.

System Node	Clock Role	Representative External Reference	Typical Device	Selection Focus
Application Processor / SoC	Main processor / PLL reference	19.2 / 24 / 26 / 38.4 MHz	Crystal / accepted external clock	XTAL vs CLKIN · CL / ESR · drive · startup · package
Cellular / Baseband / RF	RF synthesizer / shared reference	19.2 / 26 / 38.4 MHz	Crystal / shared XO / TCXO	phase noise · waveform · DC bias · source sharing
Wi-Fi / Bluetooth	Wireless fast-clock reference	24 / 26 / 38.4 / 40 MHz	Crystal / driven clock	CL / ESR or VDD / logic · harmonics · sleep behavior
GNSS Reference	Stable positioning reference	26 MHz common platform-dependent alternatives	Clipped-sine TCXO / shared RF source	total error · temperature · phase noise · load
RTC / PMIC / Always-On	Retained-time / sleep reference	32.768 kHz	Tuning-fork crystal / low-current XO	XTAL vs CLKIN · CL · ESR · startup · current
Camera Sensor / ISP	Sensor MCLK / ISP reference	24 / 27 MHz	Generated MCLK / crystal / CMOS clock	input range · duty cycle · jitter · drive
Display / Touch / Bridge	Local or forwarded REFCLK	12 / 19.2 / 24 / 26 / 27 / 38.4 MHz	Crystal / CMOS / forwarded clock	bridge mode · logic level · SSC permission
USB / PCIe / Peripheral	Interface / high-speed reference	24 MHz 100 MHz conditional	Crystal / CMOS / differential REFCLK	source direction · interface · jitter · termination

1 · Identify the Receiver

Record the exact SoC, PMIC, RF, GNSS, camera, bridge or interface part number together with the clock-pin names.

2 · Classify the Clock Domain

Separate passive crystal loops, driven CMOS inputs, clipped-sine TCXO inputs, differential REFCLK and generated clocks.

3 · Apply Electrical Constraints

Define CL / ESR / drive for crystals, or VDD / output / jitter / phase noise for active sources, plus temperature and package.

Recommended sequence: System node → clock input type → nominal frequency → crystal / XO / TCXO class → electrical limits → power state → package → final FCom configuration.

03

Frequency & Component Placement Matrix

A nominal frequency is meaningful only when evaluated with the receiving node and the clock architecture used by the mobile platform.

Frequency	Representative System Position	Applicability	Selection Interpretation
32.768 kHz	RTC / PMIC / always-on / wireless sleep	Common Always-On Reference	External tuning-fork crystal or low-current driven clock depending on the receiver topology.
19.2 MHz	Qualcomm-class AP / RF reference domain	Chipset-Specific Anchor	Apply the exact oscillator-loop or accepted clock-input requirements of the SoC / RF design.
24 MHz	AP / Wi-Fi / Bluetooth / camera / USB	Common Multi-Node Reference	May be a resonator loop, driven input or SoC-generated MCLK; placement determines the component class.
26 MHz	AP / cellular / Wi-Fi / Bluetooth / GNSS	Common RF / AP Reference	Passive crystal and clipped-sine TCXO paths are separate electrical architectures.
38.4 MHz	Wireless / RF / optional display bridge	Platform-Dependent	Review RF harmonic placement, CL / ESR and the stability definition used by the radio design.
40 MHz	Wi-Fi / Bluetooth reference	Common Wireless Reference	Confirm fast-clock input mode, source load, supply and sleep-state behavior.
12 / 27 MHz	Camera / display bridge / USB / legacy peripheral	Interface-Dependent	Use only where the exact sensor or bridge exposes that external reference.
100 MHz	PCIe / high-speed bridge / FPGA / dock	High-Speed Extension	Conditional in mobile systems; interface standard, termination, jitter band and power define the source.

19.2 / 24 MHz

Application-processor and shared system-reference anchors.

26 / 38.4 / 40 MHz

Cellular, wireless and GNSS-related reference set.

12 / 27 / 100 MHz

Conditional multimedia and high-speed interface references.

32.768 kHz

RTC, sleep and retained-time clock domain.

Reference-clock interpretation: CPU operating frequency, MIPI lane rate, display refresh rate, camera frame rate, USB data rate and GNSS update rate do not directly define the external crystal / oscillator frequency.

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Representative Platform & Architecture Matrix

Four public platforms show how 19.2 MHz, 24 MHz, 26 MHz, 32.768 kHz and peripheral references appear in handset, tablet and evaluation-board architectures.

QUALCOMM / 96BOARDS

DragonBoard 410c · Snapdragon 410 / APQ8016

1

Architecture: smartphone-class application processor, PMIC, wireless connectivity and GNSS / RF functions organized around a common XO domain.

Public clock evidence: the APQ8016 device specification identifies 19.2 MHz as the required XO frequency; 96Boards publishes the board BOM and schematic set.

19.2 MHz XO → APQ8016 / PMIC → RF / WLAN / GNSS

Selection insight: a shared 19.2 MHz domain does not identify the physical source class by itself; confirm whether the implemented node is a passive loop or a driven input.

MEDIATEK

Genio 350 EVK · MT8365

2

Architecture: integrated application-processor platform with wireless, GPS, display and camera support, representative of tablet and connected-multimedia clock trees.

Public clock evidence: MT8365 defines a 26 MHz crystal oscillator, an external 26 MHz reference / TCXO input and a 32 kHz clock domain.

26 MHz XTAL / TCXO → MT8365 PLL Tree → AP / Multimedia / I/O

Selection insight: the passive 26 MHz loop and external-TCXO input are distinct interfaces; the 32 kHz domain is assigned only where the schematic exposes an external source.

PINE64

PinePhone v1.2b · Allwinner A64

3

Architecture: open smartphone schematic with discrete SoC, Wi-Fi / Bluetooth, cellular / GNSS modem, display bridge, cameras and PMIC / RTC functions.

Public clock evidence: the A64 uses 24 MHz and 32.768 kHz; the wireless section uses a 24 MHz / 10 ppm crystal, and the digital-video section uses a 27 MHz oscillator.

24 MHz + 32.768 kHz → A64 / Wi-Fi → 27 MHz Video

Selection insight: one board can contain multiple 24 MHz crystal loops, a separate 32.768 kHz domain and a driven 27 MHz peripheral reference.

PINE64

PineTab2 · Rockchip RK3566

4

Architecture: tablet schematic with RK3566, RK817-5 PMIC / codec, MIPI camera and display, USB / PCIe and alternative Wi-Fi / Bluetooth implementations.

Public clock evidence: a 24 MHz 3225 crystal serves the RK3566; a 24 MHz / 8 pF 2016 crystal serves the BES2600 wireless device; the PMIC distributes 32.768 kHz.

24 MHz 3225 → RK3566 + PMIC → 24 MHz / 8 pF Wi-Fi

Selection insight: separate 24 MHz loops can require different packages and CL values, while PMIC-distributed 32.768 kHz avoids an unnecessary second RTC source.

Platform interpretation: these public examples illustrate representative clock placement only. They do not imply FCom adoption, approved-vendor status, certification, compatibility or drop-in approval. Final component selection should be based on the exact board revision, receiver documentation, schematic and validation results.

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SoC + Wireless + GNSS Timing Architecture

Representative external timing from the application-processor reference through wireless, GNSS and always-on domains.

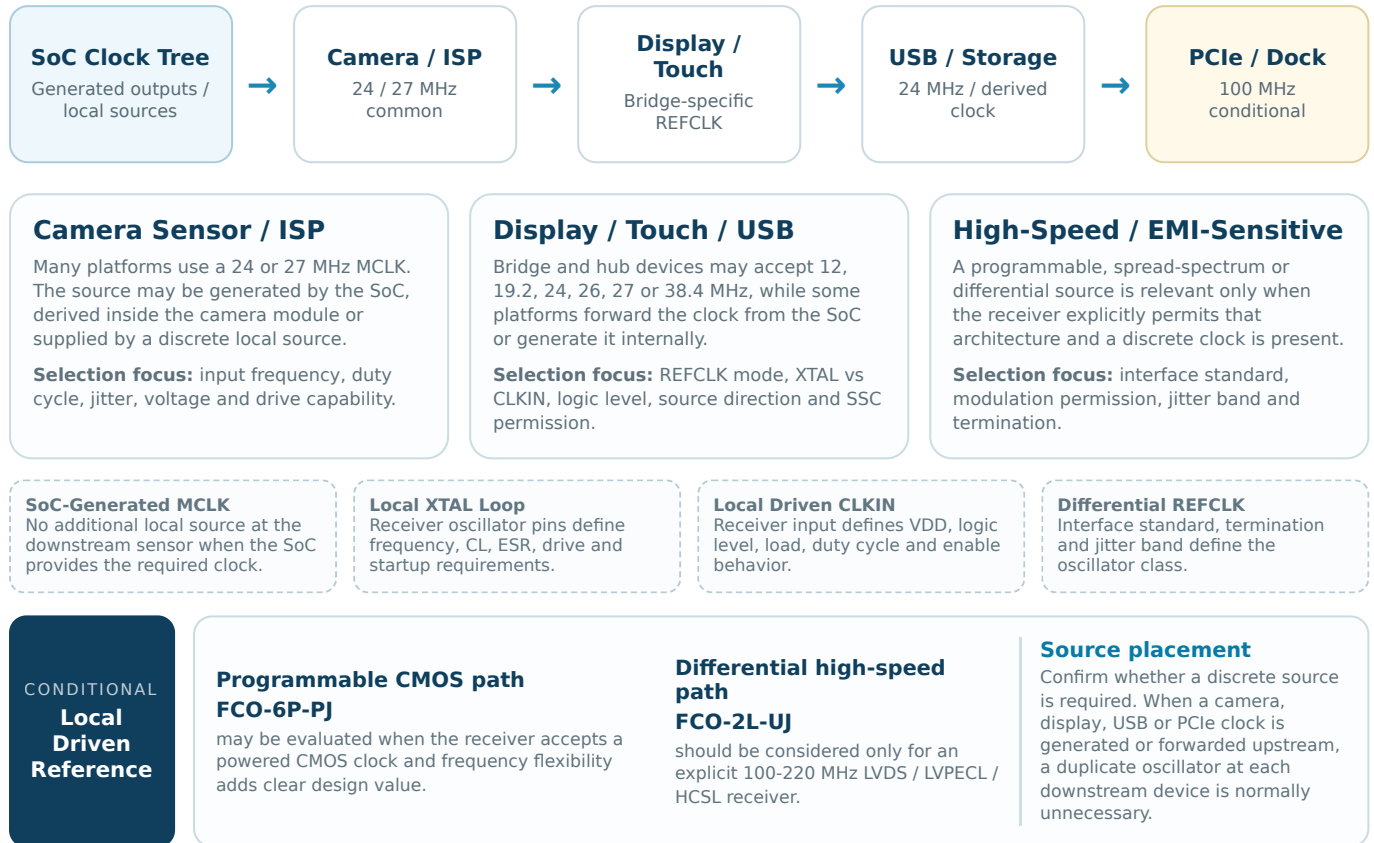


Architecture note: when the SoC, radio and GNSS chain share one qualified reference, a separate local source is typically unnecessary. Confirm buffer direction, loading and power-state behavior before assigning any local timing device.

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Camera + Display + Peripheral Timing Architecture

Representative timing around sensor MCLK, display / touch bridges, USB and optional 100 MHz high-speed references.



Architecture note: MIPI lane rate, display pixel rate and USB / PCIe data rate are not substitutes for the receiving device's documented external reference requirement.

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FCom Selection Guidance by Design Condition

The product families below address the primary timing decisions in smartphone and tablet architectures. FCom confirms the exact ordering code during application review after the receiving clock interface is defined.

SoC / Wireless XTAL

Compact external resonator path for 19.2-40 MHz-class references.

RTC / Always-On

32.768 kHz passive loop or low-current driven CLKIN.

GNSS Stable Reference

Clipped-sine TCXO where total accuracy and temperature stability are specified.

Driven Local Clock

CMOS or conditional differential reference when the node expects CLKIN.

Design Condition	FCom Selection	Selection Rationale	Key Check Before RFQ
19.2 MHz + 2016 XTAL loop	FCX-2S	Its published 16-96 MHz range makes FCX-2S a practical 2016 selection starting point for a documented 19.2 MHz passive loop.	CL · ESR · drive · startup margin · package
Space-constrained 24-40 MHz XTAL loop	FCX-1S / FCX-1M	The 1210 and 1612 alternatives offer distinct published ESR ranges for space-constrained AP / wireless loops.	Frequency · CL · ESR · drive · board loss
32.768 kHz RTC exposes XTAL pins	FCT-1S / FCT-1M	Compact passive retained-time path for RTC, PMIC, sleep and low-power wake functions.	CL 6-12.5 pF · ESR 70-90 kΩ · startup
32.768 kHz receiver expects driven CLKIN	FCO-6K-UC	Published low-current CMOS option: 2016, 1.5 / 1.8 V, ±20 ppm, -40 to +105°C and 1.4-1.8 µA current consumption.	CLKIN level · VDD · current · load · enable
GNSS / RF accepts stable clipped-sine source	FVT-6S	2016 TCXO / VCTCXO path with 10-52 MHz range, 1.8-3.3 V options, ±0.5 ppm and -40 to +85°C.	Frequency · waveform · load · phase noise · DC bias
Receiver expects local driven CMOS CLKIN	FCO-1C / FCO-6C	1612 / 2016 CMOS options for local 1.5-60 MHz-class clocks; not applicable to passive XTAL pins.	Frequency · VDD · logic · load · OE · current

Application-specific configurations: FCom application engineering can evaluate **FCT-2M-LC** for a documented 3 pF RTC loop, **FCO-6P-PJ** for a permitted programmable CMOS clock and **FCO-2L-UJ** for an explicit differential 100-220 MHz receiver. Each series should be specified only when the receiver architecture requires the corresponding condition.

ENGINEERING SELECTION SUPPORT

Request an FCom Mobile Timing Recommendation

Provide the target SoC / RF / Wi-Fi / Bluetooth / GNSS / PMIC / camera / bridge part number, clock pins, frequency, CL / ESR or supply / output, jitter / phase-noise requirement, package and project stage.

[Start Engineering Review →](#)

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Engineering Validation & Minimum RFQ

Mobile timing is defined by the receiving node, source topology, power states and RF / interface environment in addition to nominal frequency.

SoC / Baseband / Wireless

- Exact IC part number
- Clock-pin names and schematic node
- XTAL or driven CLKIN topology
- Frequency, CL / ESR or VDD / logic
- Startup / phase noise if specified
- Power-state behavior

GNSS / RF Reference

- Receiver / RF device P/N
- Local or shared reference
- Frequency and accepted waveform
- Total accuracy and temperature
- Phase-noise mask / DC bias / load
- Shielding and physical placement

RTC / Always-On

- PMIC / RTC / MCU P/N
- XTAL pins or external CLKIN
- 32.768 kHz CL / ESR or VDD / current
- Oscillator gain and startup target
- Backup-power architecture
- Timekeeping objective

Camera / Display / Peripheral

- Sensor / bridge / hub / PCIe P/N
- Local, generated or forwarded clock
- Frequency and interface standard
- VDD / logic / duty cycle / jitter
- SSC permission and termination
- Package and power budget

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	SoC, baseband, Wi-Fi / Bluetooth, GNSS, RTC / PMIC, camera, display bridge, USB, PCIe or other peripheral.
Target Device	Exact receiving IC part number, clock pin names, data-sheet section and schematic location.
Clock Topology	External resonator, local CMOS XO, shared / forwarded clock, clipped-sine TCXO, differential REFCLK or external 32.768 kHz source.
Crystal Requirements	Frequency, package, CL, ESR, tolerance / stability, drive level, startup target and operating temperature.
XO / TCXO Requirements	Frequency, VDD, output / waveform, stability, temperature, jitter / phase noise, load, OE and current.
Program Requirements	Prototype quantity, sample date, validation plan, annual volume, production location, lifecycle and compliance documentation.

Same Frequency, Different Interfaces

A 26 MHz crystal, CMOS oscillator and clipped-sine TCXO are separate electrical classes.

32.768 kHz Supports Two External Paths

RTC may use a tuning-fork crystal oscillator loop or accept a low-current driven clock input.

Generated Clocks Typically Avoid a Duplicate Source

A clock generated by the SoC, PMIC, PHY or bridge normally does not require a second local oscillator at the downstream node.

Frequency alone does not define the final part: the receiving device, clock-interface type, power state and electrical limits determine the appropriate FCom series and exact configuration.

09

Engineering FAQ & Application Review

Common mobile timing questions, representative public architecture references and the information required for FCom engineering review.

Is the SoC GHz rating the external crystal frequency?

No. The external reference feeds internal oscillator / PLL domains; CPU, GPU, memory and multimedia clocks are synthesized inside the platform.

Can a passive crystal replace a clock oscillator?

No. A crystal relies on the receiver oscillator loop. An XO is powered and drives an electrical clock output.

Are a 26 MHz crystal and 26 MHz TCXO interchangeable?

No. They differ in topology, supply, waveform, bias, load, phase noise, stability and power behavior.

Can a 32.768 kHz crystal replace a kHz XO?

Only if the receiver topology is redesigned and validated. XTAL pins and a driven 32.768 kHz CLKIN are different interfaces.

Does MIPI lane rate determine camera / display reference?

No. MIPI data rate and sensor / bridge REFCLK are separate; select the reference from the exact device documentation.

When does a 100 MHz node need a discrete source?

Only when the exact PCIe, bridge or dock architecture exposes a local REFCLK input. Confirm interface, termination, jitter and power.

Why do CL and ESR need exact confirmation?

They affect oscillation frequency, startup margin and reliable operation across voltage, temperature, process and board parasitics.

Why are SAW and crystal filters not used as clock sources?

They implement RF / IF filtering or resonance functions and are not substitutes for MHz, RTC or TCXO clock sources.

Representative Public Technical References

1. **FCom:** current product-selection data and applicable series specifications supporting the recommendations in this guide.
2. **96Boards:** DragonBoard 410c hardware documentation, BOM and schematic set.
3. **MediaTek:** MT8365 data sheet - 26 MHz XTAL / external clock and 32 kHz clock-domain evidence.
4. **PINE64:** PinePhone v1.2b schematic publication page.
5. **PINE64:** PineTab2 V2 schematic - RK3566 24 MHz, BES2600 24 MHz / 8 pF and PMIC 32.768 kHz distribution.
6. **Texas Instruments:** CC2564C - 26 / 38.4 MHz fast-clock and optional 32.768 kHz architectures.
7. **NXP:** IW416 hardware-design note - 26 / 40 MHz and optional 32.768 kHz wireless clocks.
8. **Texas Instruments:** SN65DSI86 - allowed display-bridge REFCLK frequencies.
9. **Microchip:** USB251xB - 24 MHz USB-hub reference architecture.

FCom product specification note: product information in this guide is presented at series or representative-configuration level. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom specification and quotation.

ENGINEERING REVIEW

Smartphone & Tablet Timing Review

Provide the target SoC / RF / Wi-Fi / Bluetooth / GNSS / PMIC / camera / bridge part number, clock input, frequency, CL / ESR or supply / output, phase-noise / jitter target, temperature, package and project stage. FCom application engineering can review the requirement and recommend a suitable timing series and configuration for system-level validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and applicable FCom product specification, followed by validation on the complete board and system.