

SMART TV, STREAMING & HOME AV

Smart TV, Streaming & Home AV

This guide supports the coordination of video and digital, networking, wireless, audio and retained-time clock domains across connected display and home-entertainment platforms.

Video & Digital Timing + Network Interfaces + Wireless Connectivity + Audio Timing + Retained-Time

Smart TVs

Streaming / Set-Top Boxes

Projectors / Media Players

Smart / Wireless Speakers

Soundbars

Network Audio / Home Hi-Fi

Application Scope

Application and video processors, HDMI / display paths, Ethernet PHYs, Wi-Fi / Bluetooth connectivity, audio DSPs, codecs, DACs / ADCs and external retained-time functions.

Selection Philosophy

Selection begins with the receiving clock node. Video / digital references, networking clocks, wireless references, audio MCLKs and RTC clocks are separate domains even when they coexist in one product.

Processor & Video

Application SoC, video engine and local interface references.

Network & Wireless

Ethernet PHY, Wi-Fi and Bluetooth timing.

Audio

DSP, codec, DAC / ADC and audio master clocks.

Retained- Time

RTC, standby scheduling and persistent-time functions.

01

Application Scope & Engineering Domains

Connected display and home-AV platforms combine processing, interface, network, wireless, audio and retained-time functions, each with a different external clock role.

One product, multiple timing domains. The application processor, HDMI / video path, Ethernet PHY, wireless subsystem, audio converter and RTC may each use a different reference source. Timing selection therefore begins with the receiving IC and its documented clock input.

Typical Equipment

Display & Streaming

Smart TV
Streaming Box
Set-Top Box
Projector
Multimedia Player

Connected Audio

Smart Speaker
Wireless Speaker
Soundbar
Network Audio
Home Hi-Fi

Core Interfaces

HDMI / Display
Ethernet
Wi-Fi / Bluetooth
Audio DSP / Codec
DAC / ADC

Five Engineering Domains

Processor & Video

Application SoC, video engine, decoder and system PLL references.

HDMI & Digital I/O

Video front end, display bridge and high-speed digital timing.

Network & Wireless

Ethernet PHY, Wi-Fi / Bluetooth radio and module clocks.

Audio DSP & Conversion

DSP, codec, DAC / ADC and sample-family master clocks.

RTC & Standby

Retained time, sleep scheduling and low-power system reference.

Oscillator Interface

XTAL pins · CMOS CLKIN · differential REFCLK · external RTC clock.

Frequency Accuracy

Relevant to radio, network, processor and retained-time clock budgets.

Jitter / Phase Noise

A first-order parameter in audio conversion and selected high-speed clock paths.

Product Environment

Temperature, EMI / EMC, power states, lifecycle and system validation.

Clock-definition note: CPU operating frequency, HDMI pixel / TMDS rate, Ethernet line rate, Wi-Fi / Bluetooth RF carrier, audio sample rate and amplifier switching frequency are internal or interface-domain values and are distinct from the external crystal or oscillator reference.

02

Select by System Node First

Begin with the receiving clock input, then determine frequency, device class, performance requirements and package.

System Node	Clock Role	Representative External Reference	Typical Device	Selection Focus
Application / Video SoC	Main system / PLL reference	24 / 25 / 27 MHz class platform-dependent alternatives	Crystal / CMOS XO	XTAL vs CLKIN · CL / ESR · startup · ppm · temperature
HDMI / Video Front End	Decoder / bridge / PHY support	27 MHz common 28.63636 MHz in selected architectures	Crystal / CMOS XO	device mode · clock input · accuracy · local versus shared source
Ethernet PHY	PHY reference	25 MHz	Crystal / XO	CL · ESR · drive level · accuracy · shared clocking
RMII / Driven Ethernet	Driven interface reference	50 MHz	CMOS clock / forwarded clock	source direction · clock sharing · receiver CLKIN
Gigabit / High-Speed Interface	Direct MAC / FPGA REFCLK	125 MHz only where directly exposed	CMOS / differential XO	architecture · jitter · output logic · termination
Wi-Fi / Bluetooth	Radio / baseband reference	26 / 32 / 37.4 / 38.4 / 40 MHz	Miniature crystal / XO	exact radio or module · integrated clock · CL / ESR · accuracy
Audio DSP / Codec / DAC	Audio master clock	11.2896-49.152 MHz by sample-rate family	Crystal / CMOS / low-jitter XO	MCLK ratio · input waveform · jitter / phase-noise budget
RTC / Standby	Retained-time reference	32.768 kHz	Tuning-fork crystal / kHz XO	XTAL vs driven CLKIN · CL · ESR · startup · current

1 · Identify the Receiver

Identify the processor, video receiver, bridge, PHY, radio or module, DSP, codec, DAC / ADC or RTC together with the clock pins used in the design.

2 · Classify the Clock Domain

Evaluate video / digital, network, wireless, audio and retained-time references as distinct domains before comparing timing devices.

3 · Apply Electrical Constraints

Define CL / ESR for crystals, or VDD / output / jitter for driven clocks, together with the required temperature range and package.

Recommended sequence: System node → clock input type → frequency → crystal / XO class → accuracy / jitter → temperature → package → final FCom configuration.

03

Frequency & Component Placement Matrix

Frequency becomes meaningful when it is considered together with the receiving node and the clock architecture used by the product.

Frequency	Representative System Position	Applicability	Selection Interpretation
32.768 kHz	RTC / standby / retained-time	Common Retained-Time Reference	External tuning-fork crystal or low-current driven clock depending on RTC topology.
11.2896 / 12.288 MHz	Codec / DAC / ADC / DSP MCLK	Common Audio Reference	Base audio MCLK for the 44.1 kHz or 48 kHz sample-rate family.
22.5792 / 24.576 MHz	DSP / codec / network-audio MCLK	Audio Performance Reference	Common higher-ratio audio master clocks; receiver ratios and jitter budget define the source class.
24 MHz	Application processor / peripheral controller	Common System Reference	Frequently used as an external fixed reference with higher operating clocks synthesized internally.
25 MHz	Ethernet PHY / selected system nodes	Common Network Reference	Crystal, XO and shared-clock architectures are evaluated according to the target PHY interface.
26 / 32 MHz	Wireless connectivity SoC	Chipset-Dependent	Used by selected Wi-Fi / Bluetooth architectures; exact radio or module documentation controls selection.
27 / 28.63636 MHz	HDMI / video receiver / decoder / bridge	Video Architecture Reference	Local video reference where exposed; active pixel and TMDS rates remain separate system parameters.
37.4 / 38.4 / 40 MHz	Wi-Fi / Bluetooth radio or module	Chipset-Dependent	Use only where the exact radio exposes an external oscillator loop or driven input.
45.1584 / 49.152 MHz	High-ratio audio DSP / DAC / ADC MCLK	Performance Audio Extension	Higher audio-family clocks where the receiver and clock-quality budget justify a dedicated source.
50 / 125 MHz	RMII / direct Ethernet / FPGA reference	Architecture-Dependent	May be generated, forwarded or supplied externally; clock direction and receiver interface are decisive.

24 / 25 MHz

Primary system and Ethernet external-reference anchors.

27 / 28.63636 MHz

Conditional video-front-end reference family.

22.5792 / 24.576 MHz

Core 44.1 kHz / 48 kHz audio MCLK comparison.

32.768 kHz

Retained-time and standby clock domain.

Reference-clock interpretation: HDMI data rate, Ethernet throughput, audio sample rate, Wi-Fi / Bluetooth RF carrier and processor operating frequency do not directly define the crystal / oscillator frequency. The external reference is taken from the receiving IC clock specification.

04

Representative Platform & Architecture Matrix

Four public platforms illustrate multi-clock application processing, video-front-end timing, module-integrated wireless clocks and dedicated audio-family clock generation.

NXP SEMICONDUCTORS

i.MX 8M Quad EVK · Connected Display & Multimedia Processing

1

Architecture: application processing, HDMI / multimedia interfaces and an always-on clock domain coexist on one evaluation platform.

Documented clock architecture: NXP documentation identifies distinct 25 MHz system, 27 MHz HDMI-PHY and 32.768 kHz RTC-related domains.

25 MHz System → 27 MHz HDMI PHY → 32.768 kHz RTC

Selection insight: processor, HDMI and always-on timing are separate nodes even when they are implemented on the same platform.

ANALOG DEVICES

EVAL-ADV7850 · HDMI / Video Receiver with Separate Audio Clocking

2

Architecture: HDMI and analog-video reception are combined with a separate audio master-clock path.

Documented clock architecture: the board documentation specifies a 27 MHz ± 50 ppm crystal; AC_MCLK can be supplied externally over 4.096–24.576 MHz at $128 \times f_s$.

27 MHz Video → ADV7850 Receiver → Audio MCLK

Selection insight: the video reference and audio MCLK have different sources, ratios and performance budgets.

ESPRESSIF SYSTEMS

ESP32-LyraT V4.3 · Connected-Audio Development Platform

3

Architecture: a wireless processing module connects to an external audio codec through the ESP32 I²S architecture.

Documented clock architecture: ESP32-WROVER-E integrates a 40 MHz radio / system crystal; the public board design does not show a default separate host-board audio XO.

40 MHz Module → ESP32 + I²S → Codec / Audio

Selection insight: module-integrated timing must be confirmed before an additional host-board clock is considered.

XMOS

XK-AUDIO-316-MC-AB · Multichannel USB / Network-Audio Platform

4

Architecture: a fixed system reference coexists with selectable audio master-clock generation for multiple sample-rate families.

Documented clock architecture: XMOS documents a 24 MHz external crystal and audio MCLK families at 11.2896 / 12.288 / 22.5792 / 24.576 / 45.1584 / 49.152 MHz.

24 MHz System → PLL / Clock Generation → Audio MCLK

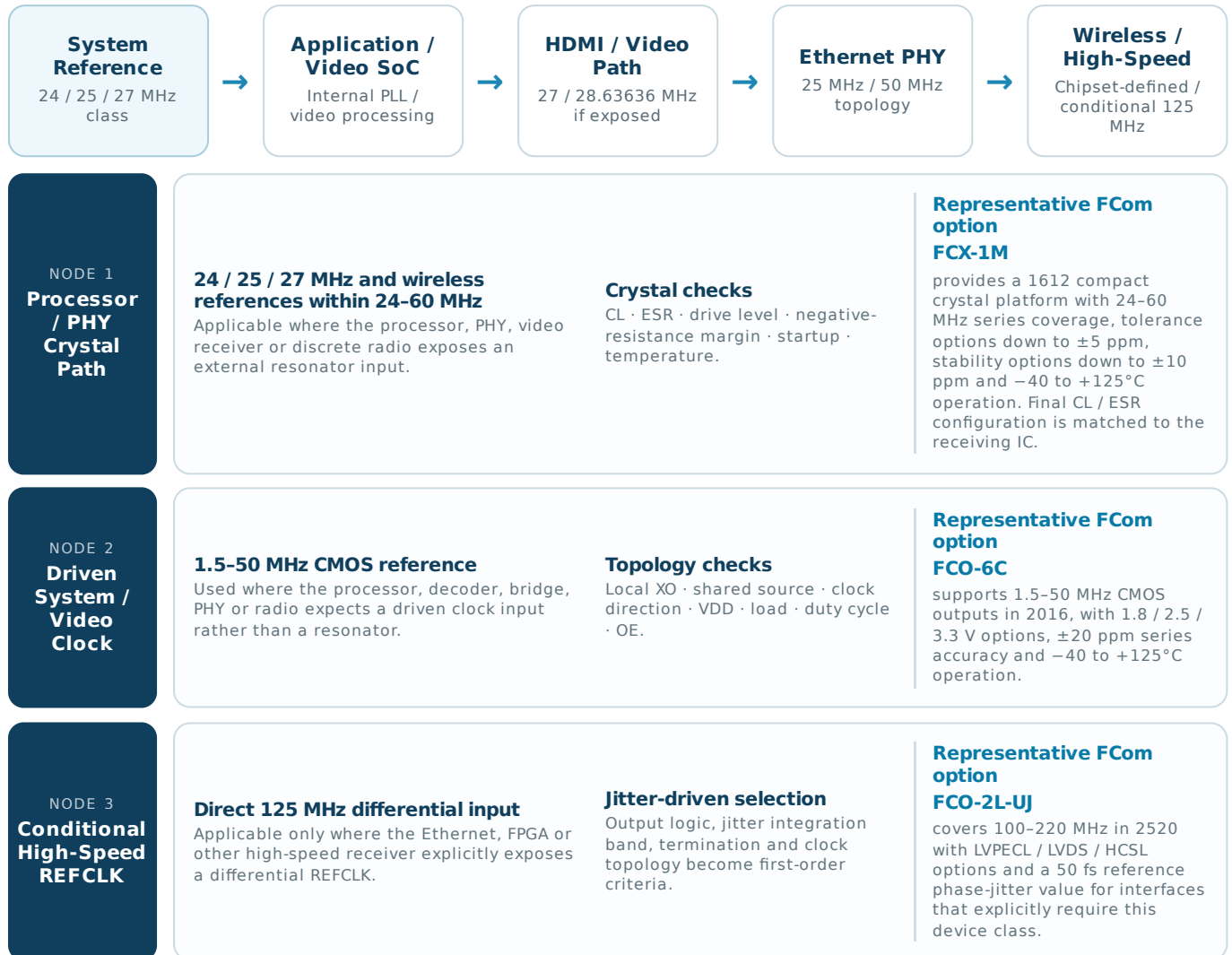
Selection insight: system timing and low-jitter audio-family timing can require separate external clock decisions.

Platform interpretation: these public examples are included solely to illustrate representative timing architectures. They do not imply affiliation, endorsement, approval, qualification, confirmed FCom design-in or drop-in compatibility. For each customer design, component selection is verified against the latest target-device documentation, schematic and complete system requirements.

05

Smart TV / Streaming Video Timing Architecture

Representative external timing from the application processor into video / HDMI, Ethernet and wireless-connectivity nodes.

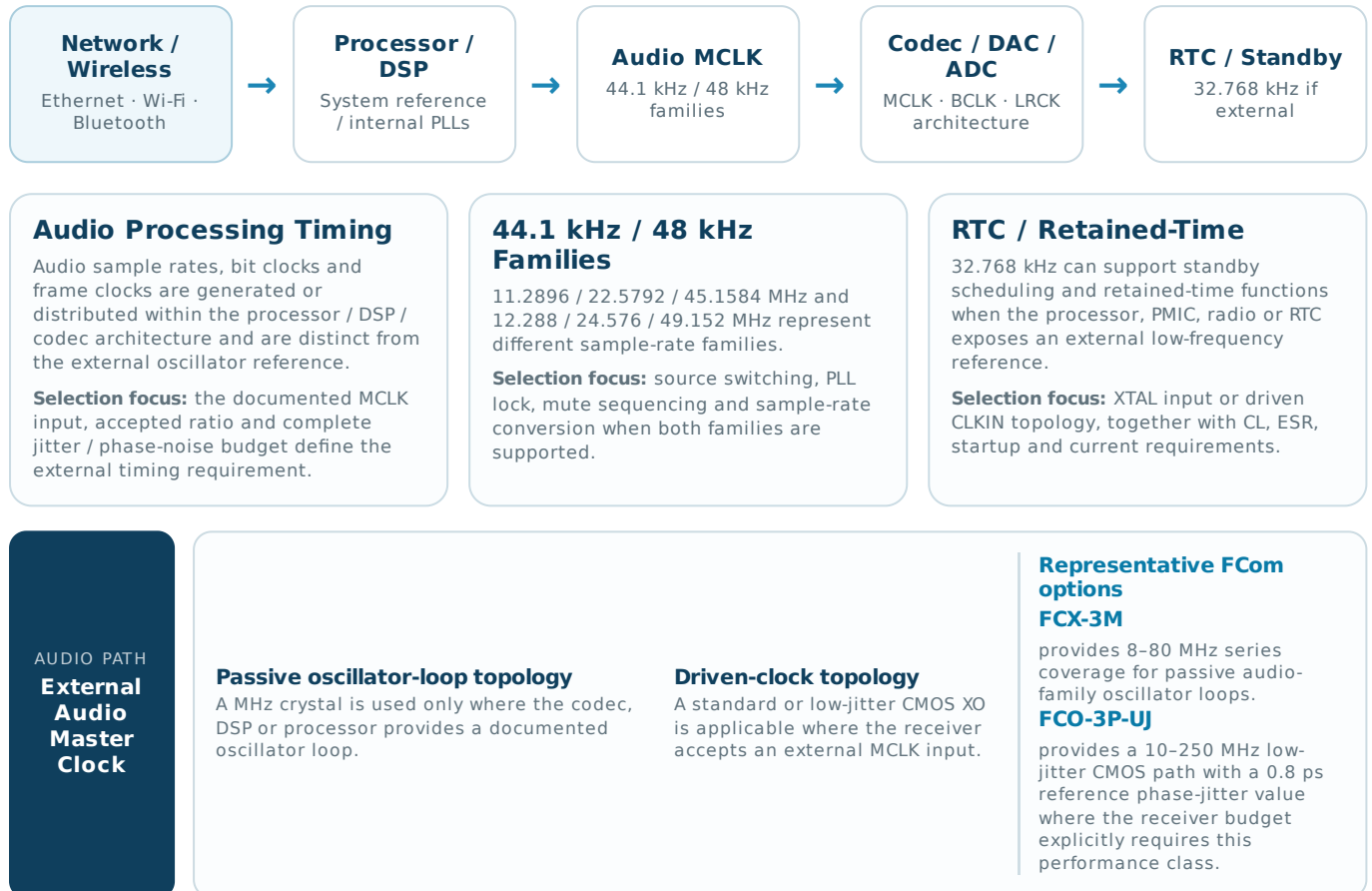


Architecture note: 50 MHz RMII and 125 MHz Ethernet clocks may be generated or forwarded by another device. The target-node topology therefore determines whether the design uses a local crystal, local XO or distributed reference.

06

Connected Audio + Retained-Time Architecture

Representative timing around network / wireless inputs, application processing, audio DSP / conversion and standby functions.



Architecture note: a low-jitter XO is not automatically required at every audio node. RTC timing is a separate clock domain, and a wireless module may already integrate its radio crystal and RF filtering.

07

FCom Selection Guidance by Design Condition

The product families below correspond to the primary timing decisions in Smart TV, streaming and home-AV architectures. Exact ordering codes are confirmed after the receiving clock interface is defined.

System / Network XTAL

External resonator input in the 24–60 MHz class.

Audio-Family XTAL

Passive codec, DSP or converter oscillator loop.

Driven / Low-Jitter MCLK

Documented CMOS clock input with standard or performance-led timing.

Retained-Time

32.768 kHz external crystal for RTC / standby functions.

Design Condition	FCom Selection	Why It Changes the Decision	Key Check Before RFQ
24–60 MHz receiver exposes XTAL pins	FCX-1M	The 1612 passive crystal path applies where the processor, PHY, video device or radio provides an oscillator loop and requires an external resonator.	Frequency · CL · ESR · startup margin · package
Audio receiver exposes a passive oscillator loop	FCX-3M	8–80 MHz series coverage includes the principal audio MCLK families while preserving a passive resonator architecture.	MCLK frequency · CL · ESR · drive · loop margin
Receiver expects driven CMOS MCLK / CLKIN	FCO-6C FCO-3P-UJ	FCO-6C addresses standard 1.5–50 MHz CMOS references; FCO-3P-UJ applies where 10–250 MHz coverage and an explicit low-jitter budget change the device class.	Frequency · VDD · load · OE · jitter band · phase noise
RTC exposes 32.768 kHz XTAL pins	FCT-1S	The 1210 tuning-fork crystal path applies to an external retained-time oscillator loop; available series options include CL 6–12.5 pF and ESR 70–90 kΩ.	RTC topology · CL · ESR · startup · backup-power behavior

Application-specific extensions: **FCO-2L-UJ** can be evaluated for a directly exposed 125 MHz differential low-jitter REFCLK; **FVC-3X** may be evaluated where a pullable clock is required. A discrete 2.4 GHz SAW candidate such as **FSF1109-2442M-79M-1.2-40** is considered only after the RF passband, impedance, pinout, matching and rejection mask are defined. MCF should be considered only for special narrowband IF architectures.

ENGINEERING SELECTION SUPPORT

Request an FCom Smart TV & Home AV Timing Recommendation

Provide the target processor / video receiver / PHY / radio or module / DSP / codec / DAC / ADC / RTC part number, clock pins, frequency, CL / ESR or supply / output, jitter requirement, temperature, package and project stage.

[Start Engineering Review →](#)

08

Engineering Validation & Minimum RFQ

Smart TV and home-AV timing is defined by the receiving node, clock topology and system environment in addition to frequency.

Processor / Video / HDMI

- Exact processor, receiver or bridge P/N
- XTAL or CLKIN interface
- Frequency
- CL / ESR or VDD / logic
- Startup / jitter if specified
- Operating temperature

Ethernet / High-Speed

- PHY / MAC / FPGA P/N
- 25 / 50 / 125 MHz topology
- Crystal, local XO or shared clock
- Clock direction and internal derivation
- Accuracy / jitter / termination requirements

Wireless / RF

- Radio IC or module P/N
- Integrated or host-board timing
- Crystal CL / ESR / drive
- Protocol band and coexistence
- RF passband / impedance / matching if discrete

Audio / RTC

- DSP / codec / DAC / ADC / RTC P/N
- Sample-rate family and MCLK ratio
- Passive loop or driven clock
- Jitter / phase-noise requirement
- RTC topology and backup-power behavior

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Smart TV, streaming box, set-top box, projector, speaker, soundbar or network-audio position; identify the exact clock / RF node and project stage.
Target Device	Exact receiving IC or module part number, relevant clock pin and schematic location.
Clock Topology	External resonator, local CMOS XO, shared / forwarded clock, differential REFCLK, recovered clock or external 32.768 kHz source.
Crystal Requirements	Frequency, package, CL, ESR, tolerance / stability, drive level, startup and operating temperature.
XO Requirements	Frequency, VDD, output logic, stability, temperature, RMS jitter / integration band, phase noise, load, OE and termination.
RF Filter Requirements	Protocol / band, passband, insertion loss, rejection mask, impedance, pinout, matching, input power and coexistence architecture.

25 MHz Can Use Different Topologies

A 25 MHz node may be a processor crystal, Ethernet-PHY crystal, driven clock input or shared oscillator output.

Audio MCLK Is Ratio-Dependent

The receiver and sample-rate family define whether 11.2896 / 12.288, 22.5792 / 24.576 or a higher MCLK is appropriate.

32.768 kHz Supports Two External Paths

RTC may use a tuning-fork crystal oscillator loop or accept a low-power driven clock input.

Frequency alone does not define the final part: the receiving device, clock-interface type and video / network / audio / RTC topology determine the appropriate FCom series and exact electrical configuration.

09

Engineering FAQ & Application Review

Common Smart TV and home-AV timing questions, representative public architecture references and the information required for FCom engineering review.

Is the HDMI pixel or TMDS rate the external oscillator frequency?

No. The external reference is defined by the processor, bridge or receiver clock input and may be independent of active video timing.

Can 44.1 kHz- and 48 kHz-family MCLKs be interchanged?

Not automatically. The codec, DAC, ADC or DSP must support the selected MCLK ratio or a defined PLL / sample-rate-conversion strategy.

Does Gigabit Ethernet always require a 125 MHz XO?

No. Many PHYs use a 25 MHz crystal or clock and derive or export 125 MHz internally.

Does a wireless module need a host-board crystal?

Not necessarily. Many modules integrate the radio crystal and RF filtering; a host-board timing device is considered only when the module exposes the corresponding clock interface.

Does a passive crystal have a phase-jitter rating?

Not in the same manner as a complete oscillator. Oscillator-loop phase noise and jitter depend on the receiving IC, crystal, power, layout and operating conditions.

When is a low-jitter XO appropriate?

When the receiver exposes a driven clock input and the DAC, ADC, codec, DSP or high-speed interface has a documented jitter budget.

Is a 2.4 GHz SAW filter always required?

No. It should be considered only where the selected RF architecture includes a discrete filter position matching the required passband and rejection mask.

Is an MCF a standard Smart TV / Home AV part?

No. An MCF should be considered only for a special narrowband IF or dedicated receiver chain with a defined center frequency and bandwidth.

Representative Public Technical References

1. **NXP**: i.MX 8M Quad Evaluation Kit product page.
2. **NXP**: i.MX 8M Quad / DualLite / Dual processor data sheet and clock requirements.
3. **Analog Devices**: UG-420 EVAL-ADV7850 evaluation-board user guide.
4. **Espressif**: ESP32-LyraT V4.3 development-board guide.
5. **Espressif**: ESP32-WROVER-E / WROVER-IE module data sheet.
6. **XMOS**: xcore.ai multichannel-audio board hardware manual.

FCom product specification note: product information in this guide is presented at series or representative-configuration level unless a complete SAW filter P/N is shown. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

Smart TV, Streaming & Home AV Timing Review

Provide the target processor / video receiver / PHY / radio or module / DSP / codec / DAC / ADC / RTC part number, clock input, frequency, CL / ESR or supply / output, jitter target, operating temperature, package and project stage. FCom engineering support can review the requirement and recommend a suitable timing series and configuration for system validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.