

RF & MICROWAVE MEASUREMENT

Signal & Spectrum Analyzers

RF and microwave analysis platforms requiring low-noise references, accurate local-oscillator generation and, in selected architectures, RF / IF filtering.

Low Phase Noise + Frequency Accuracy + Converter Clock Integrity + RF / IF Selectivity

Spectrum Analyzers

Vector Signal Analyzers

Real-Time Spectrum Analyzers

RF Analyzers

EMI Receivers

Phase Noise Analyzers

Application Scope

RF / microwave instruments that translate, digitize and analyze spectral content using precision references, LO / synthesizer chains, high-speed acquisition and digital processing.

Selection Philosophy

Select by system node first. Master reference, PLL / LO reference, ADC clock, local digital clock, RF preselection and narrowband IF nodes serve different functions and should be evaluated as distinct engineering domains.

Reference

10 MHz-class precision reference, stability, aging and close-in phase noise.

LO / Synthesizer

Reference purity, tunability, PLL multiplication and spurious performance.

Conversion

ADC / converter clock jitter, differential interface and wideband acquisition.

RF / IF Filtering

RF preselection and high-Q analog IF filtering where the receiver architecture calls for them.

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Application Scope & Engineering Domains

Separate frequency-reference quality, LO generation, converter clocking and analog filtering before assigning an FCom product family.

Analyzer performance is hierarchical. A platform may use a 10 MHz precision reference, one or more PLL / synthesizer stages, a 100 MHz-class board reference and a substantially different converter sample rate in the same instrument.

Typical Equipment

Spectrum Analysis

Swept Spectrum Analyzers
Real-Time Spectrum Analyzers
RF Analyzers
EMI Receivers

Vector Analysis

Vector Signal Analyzers
Wireless Signal Analyzers
Modulation Analyzers
Wideband IQ Analysis Platforms

Low-Noise Measurement

Phase Noise Analyzers
Frequency Stability Analyzers
Specialized RF Measurement Receivers
Low-Noise Downconversion Systems

Four Engineering Domains

Precision Reference

Frequency accuracy · temperature stability · aging · close-in phase noise.

LO / Synthesizer

Reference purity · phase-noise multiplication · spurs · tuning architecture.

ADC / Digital IF

RMS jitter · converter SNR · differential clocking · FFT / DSP acquisition.

RF / IF Selectivity

Preselection · passband · insertion loss · stopband rejection · high-Q IF.

FCom Timing Core

Use a **low-noise OCXO** / **high-stability TCXO** for the precision-reference domain and a **low-jitter differential XO** for converter-clock nodes. Exact series selection follows the required stability, phase noise, jitter, output interface and temperature range.

Filtering Architecture

SAW and MCF solutions are architecture-dependent. Direct-downconversion and wideband digital-IF platforms can move much of the channel-selection function into the ADC + FPGA / DSP domain.

JITTER-LIMITED CONVERTER SNR

$$\text{SNR}_{\text{jitter}} \approx -20 \log_{10}(2\pi \cdot f_{\text{IN}} \cdot t_{\text{J}})$$

As analog input frequency increases, sampling-clock jitter becomes increasingly important. Converter-clock selection should therefore be validated against the actual input-frequency range and measurement-SNR target.

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Select by System Node First

Identify whether the node is the master reference, PLL / LO reference, converter clock, local digital clock, RF preselector or narrowband IF.

System Node	Typical Function	Representative Frequency	Preferred Device Class	Selection Focus
Master Reference	Instrument accuracy / LO root	10 MHz class	Low-phase-noise OCXO	ppb stability · aging · close-in phase noise
Ovenless Precision Ref.	Compact / lower-power reference	5–52 MHz	High-stability TCXO	±50 ppb · warm-up / power tradeoff · temperature
PLL / Tunable Reference	Loop control / calibration trim	10–250 MHz	VCXO / tunable reference	Pullability · control range · phase noise
ADC / Converter REFCLK	Sampling clock tree input	100–220 MHz	Low-jitter differential XO	50 fs class · LVDS / LVPECL / HCSL · jitter budget
High-Frequency Diff. Clock	Selected converter / FPGA node	10–1500 MHz	Wide-range differential XO	Direct-clock requirement · 0.6 ps class · interface
Local FPGA / MCU Clock	Control / processing clock	1.25–125 MHz / 8–80 MHz	Quartz crystal / CMOS XO	Cost · ppm stability · temperature · load
RF / High-IF Filter	Preselection / channel filtering	110 MHz–3.55 GHz available coverage	SAW bandpass filter	Center · BW · IL · rejection · package
Narrowband IF	High-Q analog channel selectivity	21.4 / 21.7 / 45 MHz	MCF crystal filter	kHz passband · shape factor · attenuation

Reference First

Establish the master reference phase-noise and stability requirement before optimizing downstream synthesizer or converter clocks.

Clock the Node, Not the Sample Rate

ADC sample rate is not automatically the discrete oscillator frequency. Confirm the actual CLKIN / REFCLK and whether a PLL or divider sits between.

Filter Only by Architecture

Select SAW or MCF solutions after the signal path, center frequency, bandwidth, stopband mask and impedance are defined.

Recommended selection sequence: System node → actual clock / filter location → frequency → phase-noise / jitter / selectivity target → output / impedance → temperature / package → FCom series and configuration.

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Frequency & Component Placement Matrix

Keep the industry-common 10 MHz reference separate from representative converter clocks and platform-specific RF / IF frequencies.

10 MHz

CORE PRECISION REFERENCE
Low-phase-noise OCXO; high-stability TCXO where oven power / warm-up is not justified.

100–220 MHz

LOW-JITTER CLOCK DOMAIN
Low-jitter differential XO for ADC / FPGA / clock-tree reference nodes.

10–250 MHz

TUNABLE REFERENCE RANGE
VCXO where the PLL / calibration loop requires controlled pullability.

10–1500 MHz

HIGH-FREQUENCY EXTENSION
Wide-range differential XO for selected direct-clock nodes; validate the complete jitter budget.

Frequency Class	System Position	Representative Role	Preferred Device Type	Engineering Focus
CORE 10 MHz	Master / external reference	Instrument accuracy, synthesizer root and synchronization	Low-phase-noise OCXO / high-stability TCXO	ppb stability · aging · close-in phase noise
REPRESENTATIVE 100 MHz	ADC / converter reference	Board-level low-jitter clock input	Low-jitter differential XO	RMS jitter · logic standard · PLL multiplication
ARCHITECTURE 125 / 156.25 / 200 MHz	FPGA / SerDes / converter clock	Selected high-speed reference nodes	Low-jitter XO / differential XO	Clock-node requirement · interface · jitter budget
SELECTED IF 21.4 / 45 MHz	Narrowband analog IF	kHz-class high-Q selectivity	MCF crystal filter	Passband · ripple · insertion loss · attenuation
PLATFORM-SPECIFIC 300 / 460 / 877 / 1875 MHz class	Analog IF / RF channel path	Selected architecture-specific bandpass examples	SAW / RF bandpass filter	Exact center frequency · BW · stopband mask
DERIVED ADC sample rate / LO output	Internal conversion / processing	PLL, divider, DDS, DDC or synthesizer generated	Select the upstream reference node first	Confirm the discrete oscillator frequency from the actual clock node rather than from the published sample rate

Narrowband Analog IF

FCom offers MCF options in the 21.4 / 21.7 / 45 MHz class for kHz-bandwidth analog IF designs. Specific model selection follows the required IF frequency, passband, attenuation and termination.

RF / High-IF Bandpass

FCom SAW filter coverage spans 110 MHz to 3.55 GHz in the current product portfolio. The final P/N is selected from the required center frequency, bandwidth, insertion loss, stopband mask, impedance and package.

Selection note: a matching center frequency is a useful preliminary selection reference. Final RF / IF filter selection should be based on the complete passband, stopband, impedance, insertion-loss and package requirements.

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Representative Platform & Architecture Matrix

Four public analyzer platforms illustrate how the balance between precision reference, LO quality, ADC clocking and analog filtering changes with receiver architecture.

KEYSIGHT

N9042B UXA · Wideband mmWave Analysis

1

Architecture: high-performance swept / vector / real-time signal analysis with wideband acquisition and RF preselection.

Public evidence: up to **4 GHz analysis bandwidth**; Keysight calibration documentation also uses the analyzer **10 MHz reference output** for synchronized test setups.



Design implication: keep the 10 MHz precision-reference domain separate from wideband acquisition and RF-preselection decisions.

ROHDE & SCHWARZ

FSWP · Cross-Correlation Phase-Noise Analyzer

2

Architecture: dual independent receive paths, analog I/Q downconversion, ADC / FPGA processing and cross-correlation.

Public clock evidence: the published architecture uses **16-bit ADC channels at 100 MSamples/s** and intentionally separates reference / clock contributions between the two receive paths.



Design implication: low-noise references and converter-clock quality directly affect a phase-noise analyzer's measurement floor.

TEKTRONIX

RSA600A · Real-Time Digital-IF Analyzer

3

Architecture: RF conversion into a digitized IF followed by real-time IQ / FFT processing.

Public clock evidence: **40 MHz IF bandwidth, 14-bit 112 MS/s ADC**; external reference accepts each integer MHz from 1 to 20 MHz, therefore including 10 MHz.



Design implication: an external reference, IF bandwidth and ADC sample rate belong to different timing layers; the discrete oscillator frequency should be confirmed from the actual clock node.

ANRITSU

MS2850A · Wideband Digital-IF / FFT Analyzer

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Architecture: RF / microwave front end, frequency conversion, wideband digital IF, high-speed digitization and FFT / IQ processing.

Public evidence: up to **1 GHz analysis bandwidth**; Anritsu external-mixer documentation identifies a **1.8755 GHz high-IF class** for MS2840A / MS2850A-class systems.



Design implication: wideband digital-IF architectures shift value toward reference / ADC clock quality; high-IF filtering remains architecture dependent.

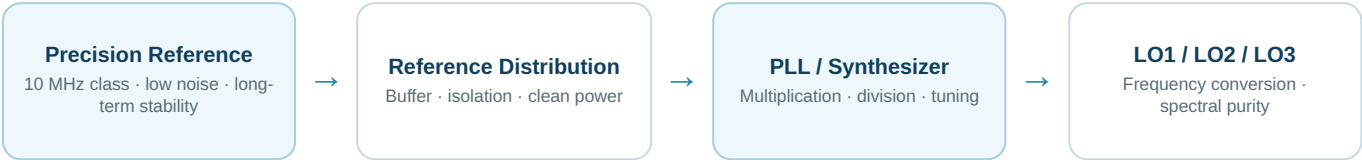
Platform reference note: These third-party platforms are included solely as publicly documented architecture references and do not imply the use, qualification or endorsement of FCom components in those instruments.

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Precision Reference & LO / Synthesizer Architecture

Build the LO chain from the measurement noise budget backward: reference stability and close-in phase noise establish the root quality before PLL multiplication and LO generation.

Representative Signal & Timing Path



LAYER 1 Maximum Reference Purity	10 MHz class Primary analyzer reference, calibration anchor and synthesizer root.	Low Noise + ppb Stability Use when close-in dynamic range, residual phase noise or long-term frequency accuracy are performance-critical.	FOC-5S-LN 14×9 · 10–40 MHz · 3.3 / 5 V · ±5 ppb · –40 to +85°C · phase noise –120 / –145 / –157 / –162 dBc/Hz @10 Hz / 100 Hz / 1 kHz / 10 kHz.
LAYER 2 Ovenless Precision	5–52 MHz Precision reference where size, power, warm-up or thermal loading argue against an oven.	±50 ppb Class Suitable only when the analyzer reference budget can accept TCXO-class stability.	FVT-7S-HP 7050 · 5–52 MHz · 2.5 / 3.3 V · ±50 ppb · –40 to +105°C · clipped sine / CMOS · –130 / –145 / –154 dBc/Hz @100 Hz / 1 kHz / 10 kHz.
LAYER 3 Tunable PLL Reference	10–250 MHz Use where the PLL, calibration loop or clock-discipline function requires analog frequency control.	Pullability Use a VCXO when the PLL, calibration or clock-discipline loop requires a pullable discrete reference.	FVC-3P-LJ 3225 · CMOS · 2.5 / 3.3 V · ±25 to ±50 ppm stability · ±50 to ±150 ppm pullability · –40 to +105°C.

LO-chain guidance: the final LO noise is a system result. Reference noise, PLL transfer, multiplication factor, VCO noise, power integrity and spurious mechanisms should be evaluated together.

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RF / IF Filtering & Digital Acquisition Architectures

Three common receiver approaches show why SAW, MCF and low-jitter clocks occupy different positions depending on how much filtering remains in the analog domain.

A · RF Preselection / High IF

RF IN → Attenuator → SAW / RF Filter → Mixer → IF / ADC

Use where fixed sub-bands or defined analog IF channels require rejection before conversion.

FCom SAW Filter Family

Current FCom coverage spans 110 MHz to 3.55 GHz. The full P/N is selected from the required center frequency, bandwidth, insertion loss and stopband mask.

B · Narrowband Analog IF

Mixer → IF Amp → MCF → ADC → DSP

Use where kHz-class analog selectivity and a deliberately narrow IF are retained before digitization.

FCF-7M

21.4 / 21.7 / 45 MHz available frequency classes. Final model selection depends on passband, attenuation and termination.

C · Wideband Digital IF / Direct Conversion

RF / Mixer → High-Speed ADC → DDC / FPGA → Digital Filter / FFT

In wideband digital-IF architectures, much of the channel selection may be performed digitally, making the precision reference and low-jitter converter clock the primary timing considerations.

Converter Clock Layer

CLOCK 1
Low-Jitter
REFCLK

100 / 125 / 156.25 / 200 MHz class

Representative board-level reference nodes for ADC / FPGA / clock-tree applications.

Differential Timing

Use the receiving converter / FPGA clock-input requirement and system jitter budget to choose interface and frequency.

FCO-3L-UJ

3225 representative low-jitter differential XO · 100–220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · ±20 ppm · –40 to +125°C · 50 fs. Package alternatives are available where required.

CLOCK 2
High-Frequency
Extension

Up to 1.5 GHz

Selected direct differential clock nodes above the ultra-low-jitter family range.

Architecture Specific

Applicable when the receiving device is designed for a directly supplied high-frequency external reference.

FCO-3L-PG

3225 · 10–1500 MHz · 2.5 / 3.3 V · LVPECL / LVDS · ±25 ppm · –40 to +105°C · 0.6 ps.

Filter selection: center-frequency compatibility is only the first step. Final SAW / MCF selection requires the actual passband, stopband, impedance, insertion-loss budget, package and temperature range.

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FCom Selection Guidance by Design Condition

Representative in-sale FCom series are mapped only to analyzer nodes where their stability, jitter, tuning or filtering characteristics materially affect the measurement architecture.

Precision Reference

OCXO / high-precision TCXO selected by phase noise, stability, warm-up and power.

Low-Jitter Converter REFCLK

100–220 MHz differential family with 50 fs class jitter.

High-Frequency Extension

Direct differential clock to 1.5 GHz where the receiving-device budget permits.

RF / IF Selectivity

SAW by exact filter mask; MCF only for narrowband analog IF.

Design Condition	Representative FCom Series / Model	Key Specifications	Selection Relevance
10 MHz-class master reference: phase noise / stability first	FOC-5S-LN	14×9 · 10–40 MHz · 3.3 / 5 V · ±5 ppb · –40...+85°C · phase noise to –162 dBc/Hz @10 kHz.	Primary choice when the reference directly limits close-in spectral purity or long-term accuracy.
Ovenless precision reference	FVT-7S-HP	7050 · 5–52 MHz · 2.5 / 3.3 V · ±50 ppb · –40...+105°C · clipped sine / CMOS.	Use when oven power / warm-up is undesirable and TCXO-class stability meets the instrument budget.
100–220 MHz low-jitter differential REFCLK	FCO-3L-UJ	3225 representative · LVPECL / LVDS / HCSL · ±20 ppm · –40...+125°C · 50 fs .	Representative ADC / FPGA / clock-tree reference. Package alternatives can be selected after the electrical node is fixed.
Special architecture: tunable or higher-frequency direct clock	FVC-3P-LJ / FCO-3L-PG	VCXO: 10–250 MHz with ±50 to ±150 ppm pullability. Wide-range differential XO: 10–1500 MHz, LVPECL / LVDS, 0.6 ps class.	Applicable when the design requires voltage control or a direct clock above the ultra-low-jitter family range.
Analog RF / IF filtering	FSF series / FCF-7M	SAW selected by full RF / IF mask; MCF for selected narrowband 21.4 / 21.7 / 45 MHz-class analog IFs.	Full filter P/N selection should be based on the complete filter mask rather than center frequency alone.

Supporting local clocks: standard quartz crystal or CMOS XO solutions can be used for MCU / FPGA / housekeeping nodes where the target IC does not require precision-reference or ultra-low-jitter performance. Keep these supporting clocks out of the main application-selection path.

ENGINEERING SELECTION SUPPORT

Request an FCom Analyzer Timing / RF Review

Provide the analyzer node, reference / clock frequency, output interface, phase-noise or jitter target, RF / IF bandwidth, temperature range and prototype / production requirement.

[Start Engineering Review →](#)

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Engineering Validation & RFQ Checklist

Translate the measurement-performance target into reference, converter-clock and RF / IF filter requirements before final product and ordering-code selection.

Precision Reference / LO

- Nominal reference frequency
- Required frequency stability / accuracy
- Close-in phase-noise mask by offset
- Aging / drift requirement
- Supply / waveform / output level
- Warm-up / thermal constraints
- External-reference / calibration architecture

ADC / Converter Clock

- Exact ADC / clock-device P/N
- Actual clock-input frequency
- Maximum RF / analog input frequency
- Target SNR / ENOB
- RMS jitter target and integration band
- LVDS / LVPECL / HCSL / CMOS
- Direct vs PLL-generated clock

SAW Filter

- Center frequency
- Passband / 3 dB bandwidth
- Insertion loss / ripple
- Stopband frequencies and rejection
- Impedance / termination
- Package / temperature
- Prototype qty / EAU

MCF Crystal Filter

- IF frequency
- Required kHz passband
- Shape factor / stopband
- Insertion loss / ripple
- Guaranteed attenuation
- Termination / package
- Temperature / catalog or custom requirement

Minimum RFQ Information

Information Category	What to Provide
Instrument / Platform	Spectrum analyzer, VSA, real-time analyzer, phase-noise analyzer, EMI receiver or specialized RF measurement platform.
Target System Node	Master reference, PLL reference, LO reference, ADC / FPGA clock, RF preselector, first / second IF, or local clock.
Frequency Plan	Reference frequency and separately the LO / IF / converter / processing frequencies if different.
Performance	Stability, aging, phase-noise mask, RMS jitter integration band, SNR / ENOB or RF / IF rejection targets.
Electrical / RF Interface	VDD, output logic, control voltage / pullability, impedance, source / load termination and enable requirements.
Environment	Operating temperature, thermal / warm-up constraints, enclosure / airflow and lifecycle requirements.
Program	Prototype quantity, sample date, EAU, production location and qualification / documentation requirements.

Converter-clock guidance: include the maximum RF / analog input frequency—not only the ADC sample rate. **Filter-selection guidance:** include the full passband and stopband mask—not only the center frequency.

09

Engineering FAQ & Application Review

Common interpretation questions for signal and spectrum analyzer timing, LO, converter-clock and filtering architectures.

Is 10 MHz really the main analyzer reference?

It is the most consistently documented cross-platform precision-reference frequency. Internal PLL, LO, converter and IF frequencies remain architecture dependent.

Is the ADC sample rate the oscillator frequency?

Not necessarily. A clock PLL, multiplier or divider may generate the converter clock. Select the discrete oscillator from the documented CLKIN / REFCLK requirement.

When should an OCXO be preferred?

When reference phase noise and ppb-level stability materially affect close-in measurement, residual phase noise, long-term accuracy or calibration performance.

When is a high-stability TCXO more appropriate?

When oven power, warm-up or thermal design is undesirable and the instrument can meet its requirement with TCXO-class compensated stability.

Does every analyzer need a SAW filter?

No. RF preselection and analog IF filtering are architecture dependent. Wideband digital-IF and direct-conversion instruments may perform much of the channel filtering after ADC conversion.

When does MCF make sense?

When a deliberately narrow analog IF requires kHz-class high-Q selectivity before the ADC / DSP. This is most appropriate for selected analog-IF architectures rather than wideband digital-IF designs.

Representative Public Technical References

1. **Keysight:** N9042B UXA — wideband signal-analysis platform and real-time / preselected measurement architecture.
2. **Rohde & Schwarz:** FSWP architecture — direct downconversion, dual paths, ADC / FPGA processing and cross-correlation.
3. **Tektronix:** RSA600A Series — digital-IF architecture, 40 MHz IF bandwidth, 14-bit 112 MS/s ADC and external-reference options.
4. **Anritsu:** MS2850A — wideband signal analyzer with up to 1 GHz analysis bandwidth and digital-IF / FFT processing.

FCom product-selection note: Representative FCom products and performance figures in this guide are provided for application-selection guidance. Final frequency options, ordering codes and guaranteed electrical limits should be confirmed in the applicable FCom datasheet and project quotation.

ENGINEERING REVIEW

Signal & Spectrum Analyzer Timing / RF Review

Share the reference, LO / PLL, converter and RF / IF signal-chain architecture together with frequency, phase-noise, jitter, bandwidth, rejection, temperature and interface requirements. FCom can review the node hierarchy and recommend an appropriate product family and configuration.

[Request Engineering Review →](#)
[FCom Solutions](#)

Public third-party platforms are shown for architecture reference only. FCom component selection should be verified against the latest target-device documentation, the applicable FCom datasheet and complete system-level validation.