

RF, MICROWAVE & PRECISION SOURCES

Signal Generators & RF Sources

Spectrally clean and highly stable timing for RF, microwave and precision signal-generation equipment across master-reference, synthesis, DDS, converter and digital-support clock domains.

Precision Reference + RF Synthesis + DDS / Vector Clocking + Converter Timing + Coherent Multi-Channel

Bench RF / Microwave Sources

Vector Signal Generators

DDS & Synthesizers

PXI / Modular Platforms

Converter Clocking

Coherent Sources

Application Scope

RF and microwave sources combining precision timebases, PLL / VCO synthesis, DDS or vector generation, ADC / DAC conversion, FPGA processing and multi-instrument synchronization.

Selection Philosophy

Select by system node first. The device that controls long-term carrier accuracy is not necessarily the same device that minimizes converter jitter or closes a clock-cleaner loop.

10 MHz

External reference, internal master timebase and coherent laboratory synchronization.

25 / 100

DDS crystal and RF / microwave PLL reference nodes.

122.88 / 245.76

Vector, clock-cleaner, converter and JESD timing domains.

125 / 156.25+

FPGA, SerDes and digital-support differential references.

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Application Scope & Engineering Domains

Separate absolute reference quality, RF synthesis, vector conversion and digital-support timing before assigning an external frequency-control device.

Signal generators combine several clock domains. A precision 10 MHz master reference, a low-phase-noise PLL reference, a pullable clock-cleaner VCXO and a fixed low-jitter converter or SerDes clock solve different engineering problems even when nominal frequencies overlap.

Typical Equipment

Bench & Modular Sources

CW / swept RF generators
Microwave sources
PXI / AXIe source modules
Frequency-reference modules

Vector & Coherent Sources

Vector signal generators
Dual / multi-channel coherent sources
Baseband-to-RF platforms
Phase-aligned source arrays

DDS & Synthesizers

DDS evaluation platforms
Fractional-N / integer-N PLL sources
Clock-cleaner-based sources
Converter-driven waveform systems

Four Engineering Domains

Precision Reference

10 MHz REF IN / OUT and master timebase controlling accuracy, aging and coherence.

RF Synthesis

25 / 100 MHz references whose phase noise is translated through PLL / multiplier chains.

DDS / Vector

Crystal, VCXO, jitter-cleaner and ADC / DAC clock domains supporting modulation.

Digital Support

FPGA, JESD204, SerDes and control references selected from receiver requirements.

Main Technical Requirements

Stability & Aging

Initial accuracy · temperature stability · aging · warm-up · holdover.

Phase Noise

Carrier frequency · offset region · multiplication · loop bandwidth · spurs.

Jitter & Interface

Integration bandwidth · receiver mask · CMOS / LVDS / LVPECL / HCSL.

Pullability

APR · control voltage · slope · linearity · lock range · fixed vs VCXO.

Application boundary: final RF carrier frequencies, internal DDS system clocks and clock-IC-derived sampling clocks are not automatic board-oscillator requirements. Confirm the real external node before selecting a crystal or oscillator.

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Select by System Node First

Begin with the receiving IC or clock function, then select frequency, oscillator class, interface and FCom family.

Representative FCom families are shown only where they resolve a real selection branch. The final configuration remains dependent on the exact clock tree, phase-noise or jitter requirement and receiving-interface conditions.

System Node	Typical Function	Representative Reference	Typical Device	Selection Focus
External REF IN / OUT	Instrument synchronization	10 MHz 1–100 / 110 MHz on selected systems	Precision OCXO / high-stability TCXO	Accuracy, aging, warm-up, close-in phase noise, output level
Internal Master Timebase	Carrier accuracy / calibration continuity	10 MHz 20 / 25 / 40 / 50 MHz platform-dependent	OCXO / precision TCXO	ppb stability, aging, g-sensitivity, power, thermal design
DDS Crystal / REF Input	Reference before internal PLL multiplication	25 MHz 20–30 MHz crystal modes	Quartz crystal / low-noise TCXO	CL, ESR, drive, startup margin or waveform / phase noise
RF PLL / Synthesizer REFIN	High-PFD synthesis reference	25 / 100 MHz	Low-noise TCXO / XO / VCXO	Phase noise by offset, spurs, tunability, supply-noise sensitivity
Jitter Cleaner / Vector Clock	Pullable loop / coherent distribution	100 / 122.88 MHz	VCXO / fixed low-jitter XO	APR, control slope, loop bandwidth, electrical interface
ADC / DAC / JESD	Sampling / deterministic latency	122.88 / 245.76 MHz	Low-jitter XO / VCXO; often derived	Integrated jitter, phase-noise mask, SYSREF relationship
FPGA / SerDes	Digital processing / high-speed REFCLK	100 / 125 / 156.25 MHz	Differential low-jitter XO	Logic, common mode, termination, receiver jitter mask
MCU / Control	Management / communication	20–50 MHz class	Crystal / CMOS XO	Startup, CL / ESR, CMOS level, EMI and temperature

Precision-Reference Path

FOC-5S-LN / **FOC-7S** are representative 10 MHz master-reference starting points. Use **FVT-7S-WT** where the TCXO power, warm-up and temperature tradeoff is intentional.

Pullable-Clock Path

FVC-5X / **FVC-3P-LJ** / **FVC-3L-PG** are considered only when the PLL or clock-cleaner architecture requires control-voltage tuning and a defined APR.

Fixed Differential Path

FCO-2L / **3L** / **5L-UJ** are representative fixed-clock families for 100–220 MHz nodes requiring compatible LVDS / LVPECL / HCSL outputs.

Recommended selection sequence: System node → external vs derived → fixed vs pullable → frequency → stability / phase-noise / jitter class → output interface → package → FCom series → final electrical configuration.

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Frequency & Component Placement Matrix

Use each nominal frequency together with a real clock-tree position and a defined performance role.

Frequency	Typical Position	Primary Function	Reference / Applicability	Preferred Device
10 MHz	REF IN / OUT · master timebase	Accuracy / synchronization	Core External Reference	Precision OCXO / high-stability TCXO
25 MHz	DDS crystal · PLL REFIN	Board reference before multiplication	Common Board Reference	Crystal / TCXO / low-noise fixed reference
100 MHz	RF PLL · modular distribution · jitter cleaner	High-PFD / coherent reference	Core RF-Synthesis Node	Sine reference / VCXO / differential XO
122.88 MHz	Vector clock tree · converter reference	Pullable or fixed clock	Platform-Dependent	VCXO / differential low-jitter XO
125 / 156.25 MHz	FPGA · Ethernet · SerDes · JESD	Digital-support REFCLK	Common Support Clock	Differential ultra-low-jitter XO
245.76 MHz	ADC / DAC · JESD · vector sampling	Converter / clock-tree node	Platform-Dependent	VCXO / XO; frequently clock-IC derived
312.5 MHz	High-speed FPGA / SerDes	High-frequency digital support	Architecture-Dependent	Higher-frequency differential XO / VCXO
1 GHz	Coherent reference / DDS system clock	Special external or internally derived	Often Internally Derived	Dedicated distribution or synthesized clock

10 MHz Precision

FOC-5S-LN is the strongest low-noise matrix fit; FOC-7S is the compact OCXO direction. Stability, aging, warm-up and close-in noise remain separate requirements.

100–220 MHz UJ Range

FCO-2L / 3L / 5L-UJ provide the published 50 fs matrix class within 100–220 MHz for compatible fixed differential nodes.

Above 220 MHz

FCO/FVC-xL-PG provide frequency coverage, but form a separate performance class. Confirm the complete phase-noise and jitter budget before selection.

Specification discipline: phase noise requires carrier and offset; jitter requires integration bandwidth; VCXO requires APR and control range; stability must separate initial tolerance, temperature, supply/load effects and aging.

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Representative Platform & Architecture Examples

Public platforms illustrate how precision references, PLL clocks and DDS / converter domains appear in commercial and evaluation systems. FCom selection remains independent of the cited platform.

ROHDE & SCHWARZ

R&S SMB100B · RF / Microwave Source

1

Architecture: precision OCXO reference → low-noise synthesis → RF / microwave output, with external-reference routing for coherent operation.

Clock evidence: 10 MHz is the core laboratory reference; the platform supports variable external references across 1–100 MHz and optional 1 GHz synchronization.

10 MHz Timebase → Low-Noise Synthesis → RF / Microwave OUT

Selection insight: evaluate **FOC-5S-LN** / **FOC-7S** for a precision 10 MHz timebase; use TCXO only where the tradeoff is intentional.

KEYSIGHT

M9380A · PXIe CW Source

2

Architecture: M9300A frequency-reference module → 100 MHz module distribution → M9301A synthesizer → M9310A source-output module.

Clock evidence: 10 MHz OCXO master timebase, 1–110 MHz external REF IN and 100 MHz internal module clock are separate timing nodes.

10 MHz / REF IN → 100 MHz Distribution → RF Source Module

Selection insight: keep the precision timebase decision separate from the 100 MHz distribution-clock interface and noise requirements.

TEXAS INSTRUMENTS

TSG06D00EVM · Coherent RF DDS

3

Architecture: 100 MHz VCXO → LMK04828 jitter cleaner → LMX2820 synthesizer → high-speed DDS clock, with a separate 10 MHz synchronization path.

Clock evidence: 10 MHz IN / OUT and the 100 MHz pullable loop reference solve distinct synchronization and clock-cleaning functions.

10 MHz Sync → 100 MHz VCXO / PLL → Derived DDS Clock

Selection insight: consider **FVC-5X** / **FVC-3P-LJ** only after APR, control-voltage and input-level validation.

ANALOG DEVICES

EVAL-AD9910 · 1 GSPS DDS

4

Architecture: 25 MHz crystal / external reference → internal PLL multiplication → up to 1 GHz DDS system clock → NCO / DAC → filtered output.

Clock evidence: 20–30 MHz crystal mode, 25 MHz onboard reference and an external-clock option are public platform features.

25 MHz Reference → Internal PLL / DDS → DAC / Filtered OUT

Selection insight: evaluate **FCX-3M** / **FCX-2M** only after CL, ESR, drive and startup-margin review.

Platform interpretation: references illustrate public clock architectures only and do not imply FCom adoption, qualification, compatibility, certification, approved-vendor status or pin-to-pin replacement.

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Precision Bench or Modular RF Source

Representative placement where reference accuracy and close-in phase noise dominate the generated carrier.

LAYER 1 Reference Input & Timebase	External / Internal Reference Common laboratory reference and master calibration timebase.	10 MHz Primary accuracy, aging and coherent-distribution node.	FOC-5S-LN / FOC-7S Use FOC-5S-LN when low noise and ppb-class stability dominate; FOC-7S where compact OCXO size is required. FVT-7S-WT is a TCXO tradeoff.
LAYER 2 Reference Selection & Distribution	Conditioning · Switching · Buffering Reference selection, calibration control and multi-unit routing.	10 → 25 / 100 MHz Platform-dependent distribution and synthesis path.	System-Level Validation Confirm amplitude, impedance, additive noise, isolation, channel skew, cable delay and lock recovery across the complete reference path.
LAYER 3 RF PLL / Synthesizer	Fractional-N / Integer-N PLL High-PFD synthesis, VCO / YIG control and multiplication.	25 / 100 MHz Low-noise fixed or pullable reference.	FVT-5S-HP / FVC-9S-LN / FVC-5X Select from phase noise at the relevant offsets, spur budget, waveform, load and whether the loop explicitly requires tuning.
LAYER 4 Microwave Output & Coherence	VCO / YIG · Mixing · Filtering Frequency generation, leveling, attenuation and output protection.	RF / Microwave Derived Final carrier and coherent REF OUT paths.	Phase-Noise Allocation Do not assign the final carrier as a board oscillator frequency. Allocate reference noise through the PLL, multiplier and output chain.
Precision Priority Separate initial accuracy, temperature stability, aging, warm-up and holdover rather than compressing them into one ppm number.	RF-Noise Priority Specify carrier frequency and the offset region that matters. Integrated jitter alone does not prove close-in RF performance.	Coherence Priority Include channel skew, deterministic phase, reference-output buffering, cable delay and relock behavior.	

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Wideband Vector or Coherent DDS Source

Representative architecture separating the signal-generation path from synchronization, DDS, converter and digital-support clock domains.

Signal Path



Clock Path



Crystal vs Driven DDS Reference

Use a crystal only when the DDS / clock IC provides a compatible oscillator circuit. Use a driven TCXO / XO for an external-clock input.

Representative options: **FCX-3M / FCX-2M** or **FVT precision families**

Fixed vs Pullable Clock

Choose a VCXO only when the jitter-cleaner or PLL requires a defined APR and control-voltage loop.

FVC-5X / FVC-3P-LJ / FVC-3L-PG vs FCO-xL-UJ

Above 220 MHz

The 50 fs UJ value ends at 220 MHz. Treat PG families as a separate performance class.

FCO-3L-PG / FVC-3L-PG after complete budget review

Clock-tree design: separate synchronization accuracy, close-in RF phase noise, converter jitter and digital-interface integrity. One oscillator figure does not cover all four domains.

Derived-frequency rule: 245.76 MHz, 1 GHz and multi-GHz DDS clocks may be synthesized internally. Do not add a board oscillator until the actual clock-tree topology is confirmed.

07

FCom Selection Guidance by Design Condition

Representative FCom families are introduced only where stability, phase-noise, pullability, jitter or interface requirements create a meaningful selection decision.

Precision Timebase
For 10 MHz master-reference nodes requiring ppb stability and low close-in noise.

RF PLL Reference
For low-noise 25 / 100 MHz synthesis positions.

Pullable Clock
For jitter-cleaner / PLL loops with an explicit APR requirement.

Low-Jitter Fixed Clock
For 100–220 MHz differential converter / FPGA / SerDes nodes.

Design Condition	Representative FCom Series	Key Catalog Specifications	When to Use
Precision 10 MHz master timebase	FOC-5S-LN / FOC-7S	FOC-5S-LN: 14×9 · 10–40 MHz · 3.3 / 5 V · ±5 ppb · –40 to +85°C · –162 dBc/Hz @10 kHz. FOC-7S: 9×7 · ±5 ppb compact OCXO class.	Master reference, coherent laboratory synchronization and low-noise RF-synthesis timebase.
Precision TCXO tradeoff	FVT-7S-WT / FVT-5S-HP	7050 / 5032 · 10–52 MHz · 2.5 / 3.3 V · CMOS / clipped sine · ±50 ppb. WT to –40...+105°C; HP to –40...+85°C.	10 / 25 MHz reference where OCXO holdover, power and warm-up are not required.
Low-noise 100 MHz-class sine reference	FVC-9S-LN	14×9 · 40–150 MHz · 3.3 V sine · ±4.6 ppm · –40 to +85°C · –117 / –141 / –148 dBc/Hz @100 Hz / 1 / 10 kHz.	RF PLL reference candidate after waveform amplitude, load and exact-frequency confirmation.
Pullable CMOS reference	FVC-5X / FVC-3P-LJ	5032 / 3225 · 1.5–170 MHz / 10–250 MHz · CMOS · pull / APR configurations to ±50...±150 ppm by family.	100 / 122.88 / 245.76 MHz-class clock-cleaner nodes requiring tuning.
Fixed differential low-jitter clock	FCO-2L / 3L / 5L-UJ	2520 / 3225 / 5032 · 100–220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · –40 to +125°C · 50 fs listed matrix jitter.	122.88 / 125 / 156.25 MHz fixed converter, FPGA, JESD and SerDes support clocks.
Crystal / local CMOS support clock	FCX-3M / FCX-2M FCO-2C / FCO-3C	Crystals: 3225 / 2520, 8–80 / 12–66 MHz, ±5 ppm tolerance, ±10 ppm stability. CMOS XO: 1.25–125 MHz, 1.8 / 2.5 / 3.3 V, –40 to +125°C.	25 MHz DDS crystal and MCU / control support clocks after circuit-level verification.

Architecture-specific extension: FVC-3L-PG and FCO-xL-PG provide broad differential frequency coverage to 1.5 GHz, but must be treated as separate performance classes rather than automatic extensions of the 50 fs UJ family.

ENGINEERING SELECTION SUPPORT

Request an FCom Timing Recommendation

Send the exact clock node, target IC, frequency, stability, phase-noise or jitter limits, output interface, temperature, package and project stage.

[Start Engineering Review →](#)

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Engineering Validation & Selection Checklist

Confirm the clock-tree role, electrical interface, performance definition and environmental limits before final component selection.

Precision OCXO / TCXO

- Nominal frequency and calibration offset
- Temperature stability vs total error
- Aging and holdover objective
- Warm-up, power and thermal path
- Phase noise at relevant RF offsets

VCXO / Clock-Cleaner Reference

- External vs internally derived status
- Pull range and APR requirement
- Control voltage, slope and linearity
- Loop bandwidth / integrated-jitter band
- CMOS, sine, LVDS or LVPECL interface

Fixed XO / Differential REFCLK

- Receiver logic and common-mode limits
- LVDS / LVPECL / HCSL termination
- RMS-jitter integration band and mask
- Duty cycle, rise / fall and OE behavior
- Supply noise and layout isolation

Crystal / Local Support Clock

- Frequency, CL, ESR, C0 and drive level
- Initial tolerance / temperature stability
- Negative resistance and startup margin
- Crystal-input vs driven-clock topology
- Package and local operating temperature

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Bench RF source / vector generator / DDS / PXI module / coherent source; identify REF IN / OUT, timebase, PLL, clock-cleaner, converter, FPGA or control node.
Target IC / Module	Exact PLL, DDS, clock cleaner, ADC / DAC, FPGA / SerDes receiver or module part number and the relevant XTAL / CLKIN / REFCLK input.
Frequency / Electrical	Nominal external frequency, supply, output logic / waveform, amplitude, load / termination, enable behavior, control voltage and pull range.
Performance / Environment	Stability components, aging, phase-noise mask, jitter integration band, spur limits, coherence, package and operating temperature.
Project / Program	Prototype quantity, required sample date, annual volume, production timing, lifecycle and special environmental requirements.

Clock Architecture

Confirm external vs derived and fixed vs pullable before comparing families.

Measurement Definition

Align carrier, offset, integration band, logic, supply and test conditions.

Frequency Classification

Mark each frequency as core reference, support clock, conditional or internally derived.

Frequency alone is not sufficient: “100 MHz” does not define close-in phase noise, waveform, pullability, jitter bandwidth or interface. The final FCom ordering code follows the complete electrical and performance specification.

09

Engineering FAQ & Application Review

Common interpretation questions, selection boundaries and representative public architecture references.

Which FCom device is the strongest 10 MHz master-reference starting point?

FOC-5S-LN is the strongest low-noise matrix fit: 10–40 MHz, ± 5 ppb and -162 dBc/Hz @10 kHz. FOC-7S is the compact 9×7 mm OCXO option.

Should a 25 MHz DDS board use a crystal or an oscillator?

Use FCX-3M / FCX-2M only when the IC provides a compatible crystal oscillator circuit and CL / ESR / drive requirements are known. Use a driven reference when the input expects a clock.

Is a 50 fs digital XO automatically suitable for a 100 MHz RF PLL?

No. RF synthesis requires phase-noise data at the offset frequencies shaped by the PLL. Total integrated jitter and close-in phase noise describe different performance aspects.

When should a VCXO be selected at 122.88 MHz?

Only when the jitter cleaner or PLL requires a pullable loop reference. For a fixed differential clock, FCO-2L / 3L / 5L-UJ may be the better starting family.

Can the 50 fs FCO-UJ family be used at 245.76 or 312.5 MHz?

No. Its published range ends at 220 MHz. FCO/FVC-xL-PG provide higher-frequency coverage but require separate phase-noise and jitter-budget validation.

Are the public platform references approved FCom designs?

No. They illustrate public clock architectures only and do not imply adoption, qualification, compatibility, certification, approved-vendor status or replacement.

Representative Public Technical References

1. **Rohde & Schwarz:** R&S SMB100B RF and microwave signal generator.
2. **Keysight:** M9380A PXIe CW Source data sheet.
3. **Keysight:** M9380A startup guide and clock interconnects.
4. **Texas Instruments:** TSG06D00EVM coherent RF DDS platform.
5. **Texas Instruments:** TSG06D00EVM user's guide.
6. **Analog Devices:** EVAL-AD9910 evaluation platform.
7. **Texas Instruments:** LMX2594EVM reference requirements.
8. **Texas Instruments:** LMK04828 clock-tree data sheet.

FCom product specification note: product information in this guide is presented at the series or representative-configuration level. Exact ordering codes, guaranteed limits and availability should be confirmed against the applicable FCom datasheet and quotation.

ENGINEERING REVIEW

Signal Generators & RF Sources Timing Review

Share the target IC / module, exact clock node, external frequency, stability, phase-noise or jitter limits, supply / output, pullability, temperature, package and project stage. FCom can recommend an appropriate series and configuration.

Request Engineering Review



FCom
Solutions

This guide provides representative application and product-selection guidance. Final component selection should be verified against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.