

PRECISION MOTION & DETERMINISTIC CONTROL

Servo Drives, Robotics & Motion Control

Coordinate timing across motor-control processors, encoder feedback, FPGA-based motion processing and industrial networks to support precise control and deterministic multi-axis operation.

Controller Timing + Encoder Feedback + FPGA Processing + Industrial Networking + Multi-Axis Synchronization

AC Servo Drives

Industrial Robots

CNC / Machine Tools

Multi-Axis Motion

EtherCAT

Precision Positioning

Application Scope

Servo and robotic platforms combining fast current / velocity / position control, absolute or incremental feedback, FPGA / logic processing and deterministic industrial communication.

Selection Philosophy

Select by system node first. External timing devices normally sit at the motion controller, network PHY / processor, FPGA or RTC domain. PWM, servo-loop and encoder serial clocks are typically derived timing domains.

Control

Real-time MCU / DSP reference for ADC, PWM, current, velocity and position loops.

Feedback

Incremental / absolute encoder, resolver and high-speed feedback interfaces.

Processing

FPGA, motion acceleration, interpolation, capture and high-speed logic timing.

Networking

EtherCAT, Industrial Ethernet, distributed clocks and deterministic inter-axis communication.

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Application Scope & Engineering Domains

Separate motor control, feedback, processing and network timing before assigning any external crystal or oscillator.

Servo Drives, Robotics & Motion Control combines real-time control loops, position feedback and deterministic communication. The key design task is to identify the board-level external reference clock that supports these functions without confusing it with internally generated CPU, PWM, servo-loop or encoder-interface frequencies.

Typical Equipment

Servo & Motion

AC Servo Drives
Multi-Axis Servo Systems
CNC / Machine Tools
Electronic Cam / Gearing

Robotics

Industrial Robot Arms
Collaborative Robots
SCARA / Delta Robots
AMR / AGV Motion Modules

Precision Automation

Packaging Machinery
Semiconductor Equipment
Pick-and-Place Systems
Precision Positioning Stages

Four Engineering Domains

Motor-Control Timing

MCU / DSP external reference
→ PLL / clock tree → ADC,
PWM, current, velocity and
position loops.

Encoder & Feedback

Incremental / Tamagawa /
BiSS-C / EnDat / SSI / resolver
interfaces and deterministic
capture.

FPGA / Motion Processing

Interpolation, encoder
processing, protocol handling,
high-speed logic and optional
SerDes reference clocks.

Industrial Networking

EtherCAT / Industrial Ethernet
PHY and network processors
supporting synchronized multi-
axis operation.

Main Technical Requirements

Startup Margin

CL · ESR · drive level ·
negative resistance · startup
across temperature.

Frequency Integrity

Initial tolerance ·
temperature stability · aging ·
system ppm budget.

Low Jitter

FPGA / network REFCLK
jitter, output logic and
termination where explicitly
required.

Deterministic Operation

Stable local references +
synchronized communication
+ bounded feedback latency.

Frequency boundary: PWM frequency, current-loop rate, velocity / position-loop rate, MCU CPU frequency and encoder protocol clock are system timing parameters. External crystal or oscillator selection should instead follow the documented XTAL / CLKIN / REFCLK requirement of the receiving device.

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Select by System Node First

Begin with the motion-control or communication node, then choose the clock topology, frequency class and performance level.

Representative FCom series are introduced where they help translate the system architecture into a practical component choice. Final configuration depends on the target controller, PHY, FPGA and oscillator circuit.

System Node	Typical Function	Representative Reference	Typical Device	Selection Focus
Servo MCU / Real-Time DSP	Current / velocity / position control	20 / 25 MHz	MHz crystal / CMOS XO	XTAL vs CLKIN, CL / ESR, temperature, oscillator margin
Safety / Secondary MCU	Supervisory / safety control	16–40 MHz class	Crystal / CMOS XO	Qualification, stability, startup and package
EtherCAT / Industrial Ethernet PHY	Deterministic network interface	25 MHz	Crystal / XO	Crystal-input vs external-clock mode, ppm budget
RMI MAC-PHY	Externally driven network reference	50 MHz	CMOS XO	REF_CLK direction, logic level, duty cycle, source/load topology
Motion FPGA / Network Processor	Interpolation / protocol / high-speed logic	100 / 125 / 156.25 MHz	CMOS or differential XO	Output logic, RMS jitter, termination and signal integrity
RTC / Event Logging	Timestamp / maintenance / supervisory timing	32.768 kHz	Crystal / low-power XO	RTC topology, CL / ESR or standby-current budget
Encoder Interface Clock	Tamagawa / BiSS-C / EnDat / SSI transport	1–10 MHz class	Controller / FPGA generated	Interface timing and cable margin; typically generated by the controller / FPGA
PWM / Servo Loops	Power-stage and control-loop timing	Derived	Typically controller-derived timing	Generated from the controller clock tree rather than from a dedicated timing device

Crystal-Input Controller

Use a MHz crystal where the servo MCU / DSP includes a suitable oscillator circuit. Confirm frequency, CL, ESR, drive level, startup margin, temperature and qualification before selecting package size.

Driven Controller / RMI Reference

Use a CMOS XO where the receiving device requires CLKIN / REF_CLK. Supply, logic level, duty cycle, stability and temperature become the primary selection parameters.

High-Speed Differential Reference

A low-jitter differential XO becomes relevant where the FPGA / SerDes / network interface specifies differential signaling together with a defined RMS-jitter budget.

Recommended selection sequence: System node → external vs derived → crystal vs driven clock → frequency → temperature / qualification → jitter / output interface → FCom series → final electrical configuration.

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Frequency & Component Placement Matrix

Focus on actual board-level reference clocks and keep interface / control-loop frequencies in a separate derived-timing layer.

System Position	Typical Frequency	Primary Function	Reference / Applicability	Preferred FCom Direction
RTC / Event Log	32.768 kHz	Timestamp / maintenance timing	Optional External Reference	32.768 kHz tuning-fork crystal / low-power clock
Servo MCU / DSP	20 MHz	Real-time controller reference	Core External Reference	MHz crystal or CMOS XO, according to XTAL / CLKIN topology
Servo MCU / EtherCAT	25 MHz	Controller / network reference	Core External Reference	MHz crystal / XO; package selected after oscillator-margin review
RMII / External MAC-PHY	50 MHz	Driven REF_CLK	Interface-Dependent	CMOS XO
Motion FPGA / Logic	100 MHz	Processing / network reference	Architecture-Dependent	CMOS XO or differential XO, according to receiving interface
Gigabit Ethernet / FPGA	125 MHz	MAC / FPGA REFCLK	Architecture-Dependent	CMOS or differential XO; select the low-jitter class where the interface defines a tighter jitter budget
High-Speed FPGA / SerDes	156.25 MHz	SerDes / gateway REFCLK	Advanced Extension	Differential XO; select jitter class from the receiving-interface budget
Tamagawa / BiSS-C	1 / 2 / 2.5 / 5 / 8 / 10 MHz	Encoder serial interface	Controller-Generated	Select the upstream MCU / FPGA reference separately
PWM / Servo Loop / CPU	Application dependent	Internal control timing	Internally Derived	Derived timing; select the external reference at the controller or FPGA node

20 / 25 MHz Control

Primary external-reference range for servo MCU / DSP and selected EtherCAT / industrial-network nodes. Choose crystal or driven XO from the actual oscillator input architecture.

50 MHz Driven Network Clock

Treat 50 MHz as an interface-dependent RMII / REF_CLK requirement. A driven CMOS source is generally the relevant device class.

100–156.25 MHz Extension

Reserved for FPGA / high-speed network / SerDes domains. Output logic and RMS jitter determine whether standard or ultra-low-jitter differential clocking is appropriate.

25 / 50 MHz network note: 25 MHz is a common external reference for Ethernet-class PHY / controller architectures, while 50 MHz is typically associated with selected RMII driven-clock implementations. The exact PHY mode should be confirmed before choosing crystal or XO topology.

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Representative Motion Platform & Architecture Examples

Public platforms illustrate representative controller, network and feedback timing layers found in practical motion-control systems. FCom components should be selected against the electrical and environmental requirements of the final design.

TEXAS INSTRUMENTS

TIDM-02006 · Distributed Multi-Axis Servo

1

Architecture: F2838x runs position / speed loops and EtherCAT; distributed F28004x / F28002x nodes run current loops over FSI. One F2838x can manage up to 16 axes.

Clock evidence: later F2838x controlCARD implementations use a 25 MHz XTAL by default; earlier revisions used 20 MHz.

20 / 25 MHz Ref. → Central / Axis Controllers → FSI / EtherCAT / PWM Sync

Selection insight: local controller timing and deterministic inter-axis communication both contribute to synchronized motion.

RENESAS

CN032-ACSERVO · RZ/T2M Servo Platform

2

Architecture: RZ/T2M controller board + inverter + 220 V AC servo motor with Tamagawa absolute encoder; EtherCAT startup and motion-control support are provided.

Clock evidence: the public platform specifies 16 kHz switching and the RZ/T2M supports up to 800 MHz CPU operation, but these are derived / internal domains rather than external crystal frequencies.

EtherCAT / Host → RZ/T2M Motion Control → Encoder + Inverter

Selection insight: external reference selection should follow the controller-board oscillator circuit, not CPU or PWM frequency.

STMICROELECTRONICS

STEVAL-ETH001V1 · EtherCAT Servo Node

3

Architecture: STM32F767ZI motor-control MCU + NETX90 EtherCAT network controller + PMSM inverter + quadrature / RS485 encoder interfaces.

Clock evidence: the architecture exposes separate motor-control and network-processing domains; the STM32F767ZI supports an external 4–26 MHz crystal oscillator.

EtherCAT / NETX90 → STM32 Motor Control → Encoder / PMSM

Selection insight: one servo node can contain multiple independent external-clock decisions.

TEXAS INSTRUMENTS

TIDM-1011 · Tamagawa Absolute Encoder

4

Architecture: C2000 Position Manager / CLB generates the Tamagawa T-format link for absolute position feedback in industrial inverter and servo-drive systems.

Clock evidence: the public design supports a T-format interface clock up to 2.5 MHz and verifies operation over cable lengths up to 100 m.

Controller Reference → CLB / Encoder Interface → 2.5 MHz T-format

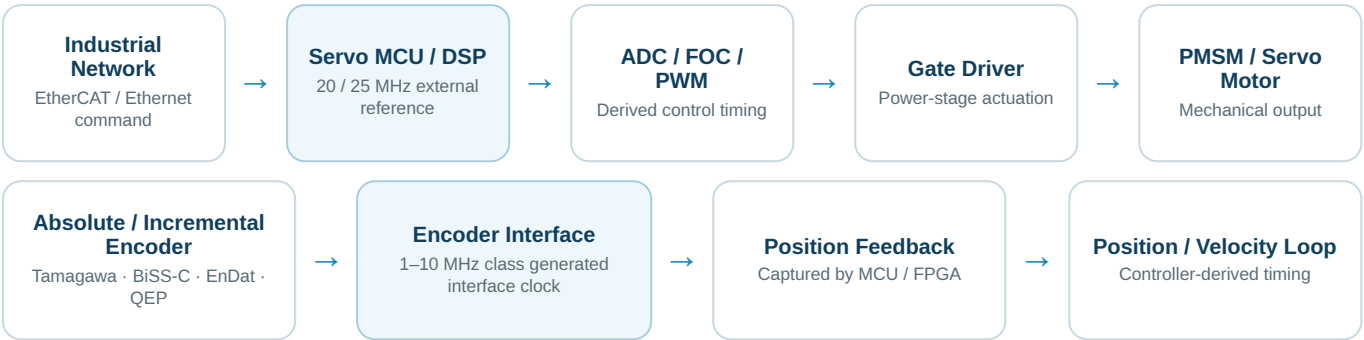
Selection insight: encoder protocol clock and external controller-reference frequency belong to different timing layers.

Platform interpretation: these examples are provided for architecture reference. FCom component selection should be verified against the exact controller / PHY / FPGA documentation, target-system schematic and complete electrical requirements.

05 Single-Axis Servo Drive Timing Architecture

Representative placement of FCom timing devices from the industrial-network reference through the servo controller and optional standby domain.

Control & Feedback Path



CLOCK 1 Servo Controller	20 / 25 MHz Representative external controller reference.	Crystal Input Use where the MCU / DSP includes a suitable oscillator circuit.	Representative FCom series: FCX-2S 2016 · 16–96 MHz · ±5 ppm tolerance · ±10 ppm stability · –40 to +125°C. An AEC-Q200 variant is available for projects with an explicit automotive-qualification requirement.
CLOCK 2 Driven CLKIN	20 / 25 / 50 MHz Controller or RMII external-clock branch.	CMOS Clock Use when the receiving device requires a driven reference.	Representative FCom series: FCO-6C 2016 · 1.5–50 MHz · 1.8 / 2.5 / 3.3 V · CMOS · ±20 ppm · –40 to +125°C.
CLOCK 3 RTC / Logging	32.768 kHz Optional maintenance log / timestamp time base.	Standby Domain Applicable where the RTC / supervisory device provides an external low-speed reference input.	32.768 kHz timing option A tuning-fork crystal is applicable where the RTC / supervisory device provides an external low-speed oscillator node. Package and qualification remain application-specific.

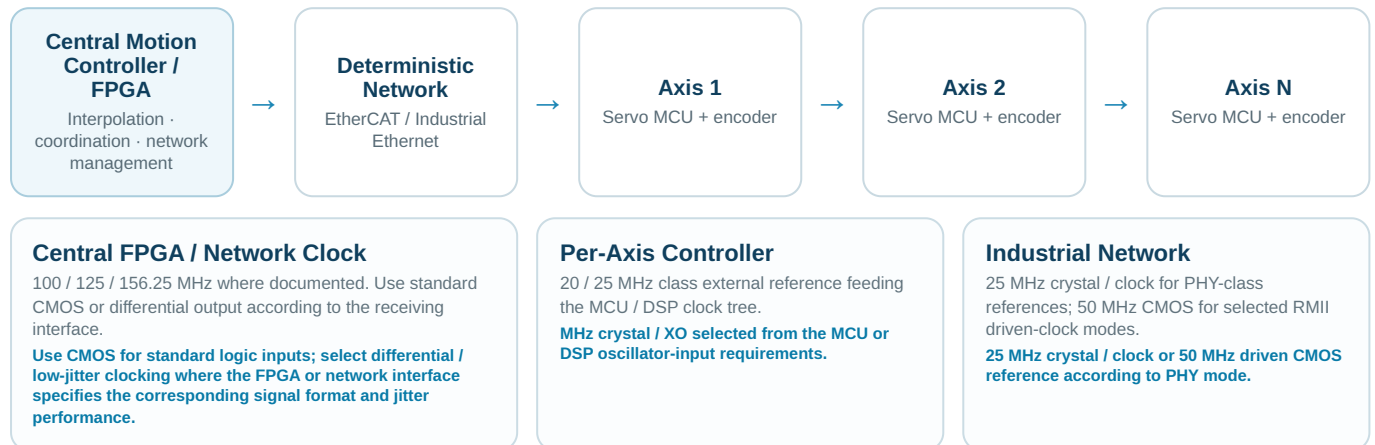
Encoder-clock rule: the 2.5 MHz Tamagawa T-format clock and BiSS-C interface clocks are generated by the controller / FPGA interface. The external reference should therefore be selected at the upstream controller or FPGA clock node.

06

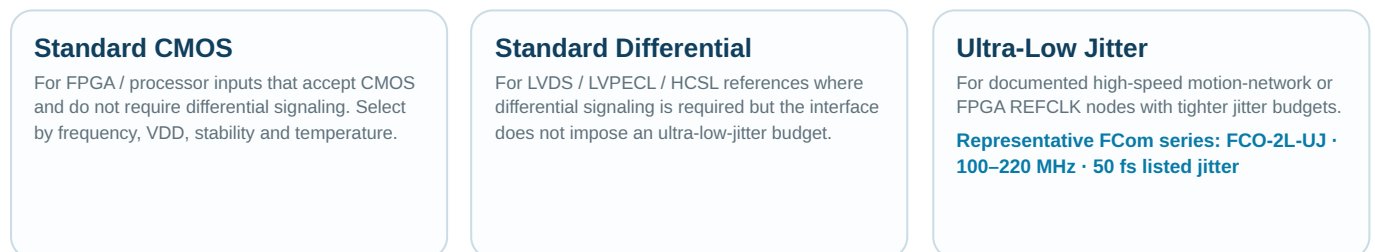
Multi-Axis Robotics & Deterministic Motion Architecture

Central motion processing, deterministic networking and per-axis servo timing must be coordinated without assuming that every internal rate requires its own external oscillator.

System Architecture



High-Speed Clock Selection



Multi-axis timing principle: deterministic motion depends on both stable local controller references and synchronized communication between axes. Network cycle time, distributed-clock correction and per-axis PWM remain separate timing layers from the physical crystal / oscillator frequency.

07

FCom Selection Guidance by Design Condition

Representative FCom series are introduced where package, clock topology, qualification, temperature or jitter creates a meaningful selection decision.

Servo Controller

20 / 25 MHz crystal or CMOS reference for real-time MCU / DSP nodes.

Industrial Network

25 MHz crystal / clock and 50 MHz driven RMII reference.

FPGA / High-Speed

100 / 125 / 156.25 MHz CMOS or differential clocking.

RTC / Supervisory

32.768 kHz timestamp / logging reference where implemented.

Design Condition	Representative FCom Series	Key Matrix Specifications	Selection Relevance
20 / 25 MHz crystal-input servo controller	FCX-2S AEC-Q200 variant available when required	2016 · 16–96 MHz · ± 5 ppm tolerance · ± 10 ppm stability · -40 to $+125^{\circ}\text{C}$ · CL 18 pF or specify · ESR frequency dependent.	Representative passive reference for real-time MCU / DSP XTAL inputs. Select the qualification level according to the project requirement.
20 / 25 / 50 MHz driven CLKIN / RMII reference	FCO-6C	2016 · 1.5–50 MHz · 1.8 / 2.5 / 3.3 V · CMOS · ± 20 ppm · -40 to $+125^{\circ}\text{C}$.	Use when the receiving controller or PHY requires an active CMOS reference.
100 / 125 / 156.25 MHz differential REFCLK with tight jitter budget	FCO-2L-UJ	2520 · 100–220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · ± 20 ppm · -40 to $+125^{\circ}\text{C}$ · 50 fs listed jitter.	High-speed FPGA / industrial-network / SerDes reference where differential signaling and low jitter are explicit requirements.
32.768 kHz RTC / event logging	FCT-2M	2012 · 32.768 kHz · ± 5 ppm · -40 to $+125^{\circ}\text{C}$ · CL 6–12.5 pF.	Optional standby / timestamp reference where the receiving device exposes an external 32.768 kHz crystal oscillator.
Harsh-environment or special-performance extension	Application-specific FCom extension	Wider-temperature CMOS, tighter-accuracy TCXO or other specialized families can be evaluated where the standard crystal / XO path does not meet the system requirement.	Provides a performance extension for designs with documented thermal, accuracy or timing requirements beyond the standard crystal / XO path.

Architecture-specific extensions: VCXO, TCXO, OCXO, Crystal Filter, SAW Resonator and SAW Filter families remain available within the wider FCom portfolio for architectures that introduce tuning, tighter temperature-compensated accuracy, holdover, RF or filtering requirements. Standard servo-controller and industrial-network clock nodes are normally addressed with crystal or XO solutions.

ENGINEERING SELECTION SUPPORT

Request an FCom Motion-Control Timing Recommendation

Send the target MCU / DSP / FPGA / PHY and exact clock pin together with frequency, CL / ESR or supply / output, temperature, jitter / stability and package requirements.

[Start Engineering Review →](#)

08

Engineering Validation & Selection Checklist

Confirm the oscillator circuit, electrical interface, network mode, feedback architecture and local environment before final component selection.

Quartz Crystal

- Frequency, CL, ESR, C0 and drive level
- Initial tolerance and temperature stability
- Negative resistance and startup margin
- Target MCU / DSP / PHY oscillator circuit
- AEC-Q200 requirement where applicable

CMOS / Differential XO

- Supply voltage and logic input requirement
- CMOS / LVDS / LVPECL / HCSL
- Duty cycle, rise / fall, OE / standby
- Jitter integration bandwidth where specified
- Termination / fan-out / signal integrity

Encoder / Feedback

- Incremental / Tamagawa / BiSS-C / EnDat / SSI
- Controller / FPGA interface device
- Interface clock rate and cable length
- Capture / latency requirements
- Confirm that interface clock is generated from the controller domain

Industrial Network

- EtherCAT / PROFINET / Ethernet architecture
- PHY / network processor exact P/N
- 25 MHz crystal vs 50 MHz RMII driven REF_CLK
- Distributed-clock / synchronization architecture
- Temperature / EMI / qualification requirements

Minimum RFQ Information

Information Category	What to Provide
Application / Motion Architecture	Servo drive / robot / CNC / positioning stage; number of axes; centralized vs distributed control.
Target IC / Node	Exact MCU / DSP / FPGA / PHY part number and XTAL / CLKIN / REFCLK / RTC pin or relevant schematic section.
Crystal Requirement	Frequency, package, CL, ESR, tolerance, stability, operating temperature, drive level and qualification.
XO / Differential Requirement	Frequency, VDD, output logic, stability, temperature, jitter target, duty cycle, OE / standby and load / termination.
Feedback / Network	Encoder protocol, network protocol, interface mode, cable length, PHY P/N and any deterministic timing constraints.
Project / Program	Prototype quantity, sample date, annual volume, production location, qualification and life-cycle expectations.

Clock Architecture

Confirm crystal-input vs driven-clock mode before comparing product series.

Timing Layer

Separate board-level reference clocks from encoder, PWM, servo-loop and CPU-derived timing.

Local Environment

Specify timing-device PCB temperature and routing proximity to inverter switching and motor-power sections.

Ordering-code note: the supplied FCom in-sale matrix provides series-level product identities and parameter envelopes. Final frequency-specific ordering suffixes should be confirmed only after the electrical configuration is defined; this guide does not invent suffixes not present in the approved matrix.

09

Engineering FAQ & Application Review

Common interpretation questions, architecture boundaries and representative public motion-control references.

Is PWM frequency the crystal frequency?

No. PWM and servo-loop rates are normally derived from the MCU / DSP clock tree. Select the external reference from the controller's documented XTAL / CLKIN requirement.

Does every encoder require an external crystal?

No. Tamagawa, BiSS-C, EnDat and similar interface clocks are commonly generated by the controller / FPGA. The upstream controller reference is selected separately.

Why are 20 MHz and 25 MHz emphasized?

They are repeatedly documented as real external controller / industrial-network references in public motion-control platforms, while many higher CPU and switching rates are internally derived.

When is 50 MHz relevant?

Primarily for selected RMI / MAC-PHY driven-clock architectures. Its applicability depends on the selected PHY / MAC interface mode rather than on Ethernet alone.

When does a low-jitter differential XO become relevant?

For documented FPGA, high-speed industrial-network or SerDes reference nodes with an explicit jitter and output-logic requirement, typically in the 100 / 125 / 156.25 MHz range.

When should a TCXO be considered?

Consider a TCXO where the required frequency accuracy over temperature exceeds the capability of the standard crystal / XO path. For most servo-controller nodes, crystal or XO solutions remain the primary architecture.

Representative Public Technical References

1. **Texas Instruments:** TIDM-02006 — distributed multi-axis servo drive over Fast Serial Interface.
2. **Texas Instruments:** C2000Ware MotorControl SDK release notes — F2838x 25 MHz default XTAL / earlier 20 MHz controlCAREDS.
3. **Renesas:** CN032-ACSERVO — RZ/T2M / RZ/T2L / RZ/N2L 220 V AC servo solution kit.
4. **Renesas:** RZ/T2M — industrial Ethernet, encoder interface and real-time servo-control MPU.
5. **STMicroelectronics:** STEVAL-ETH001V1 — EtherCAT servo-drive evaluation board.
6. **STMicroelectronics:** STM32F767ZI — external 4–26 MHz crystal oscillator support.
7. **Texas Instruments:** TIDM-1011 — Tamagawa T-format absolute encoder master interface, up to 2.5 MHz interface clock.

FCom specification basis: the complete current in-sale matrix was reviewed across Quartz Crystal Resonators, Tuning Fork Crystals, Crystal Oscillators, VCXO, TCXO, OCXO, Crystal Filters, SAW Resonators and SAW Filters. Only product families with clear motion-control selection value are included in the main path.

ENGINEERING REVIEW

Servo, Robotics & Motion-Control Timing Review

Share the target controller, FPGA, encoder interface or network device together with the exact clock node, frequency, CL / ESR or VDD / output, stability / jitter, temperature, package and project stage. FCom can review the architecture and recommend an appropriate series and configuration.

[Request Engineering Review →](#)
[FCom Solutions](#)

Public third-party platforms are shown for architecture reference only. FCom component selection should be verified against the latest target-device documentation, the applicable FCom datasheet and complete system-level validation.