

RADAR & RF SENSING

Radar & RF Sensing

Coordinate the sensor reference, FMCW clock, RF-data-converter timing and coherent master across low-power sensing, industrial radar, automotive radar and direct-RF platforms.

Stable Reference + Low Phase Noise + Sampling Integrity + Detection Sensitivity

60 GHz Presence & Ranging

76–81 GHz Automotive Radar

Industrial FMCW

Phased Array & X-Band

Direct-RF ADC / DAC

Coherent Instrumentation

Application Scope

Pulsed-coherent and FMCW sensors, 60 GHz presence / ranging modules, 76–81 GHz automotive radar, industrial monitoring, RFSOC receivers and coherent test platforms.

Selection Philosophy

Selection begins with the physical, replaceable clock node. Radar carrier, chirp PLL, crystal loop, driven reference, converter sample clock, SYSREF and serial reference are separate domains.

Sensor Reference

Passive crystal loop at the exact frequency specified by a bare radar IC.

Active FMCW Clock

Driven CMOS reference with defined jitter, duty cycle, startup and amplitude.

Converter Clock

Low-jitter differential source for RF converters, fabric and MGT references.

Coherent Master

High-stability TCXO or low-noise OCXO for an exposed system-reference path.

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Application Scope & Engineering Domains

Radar and RF-sensing systems multiply a low-frequency reference into a microwave or millimeter-wave carrier and may add independent converter and synchronization clocks.

Separate the reference, carrier and sampling domains. A 60 GHz or 76–81 GHz radar can use a 24, 38.4, 40, 50, 76.8 or 80 MHz device reference while an RFSoc platform may also expose 100–156.25 MHz board clocks and a 10 MHz coherent master.

Typical Equipment

Low-Power Radar Sensors

Presence and occupancy
Level and distance sensing
Gesture and vital-sign sensing
Smart-building radar
Battery-powered modules

Industrial & Automotive Radar

60 GHz FMCW nodes
76–81 GHz satellite radar
Robotics and safety zones
Traffic and perimeter sensing
Condition monitoring

RF Conversion & Coherent Systems

RFSoc receivers
Direct-RF ADC / DAC
Phased-array processing
Coherent instrumentation
Wideband spectrum sensing

Five Engineering Domains

Passive Radar Reference

Exact CL, ESR, drive, C0, tolerance and startup for a documented crystal loop.

Active FMCW Reference

Waveform, amplitude, duty cycle, startup, OE, jitter and supply-noise limits.

Converter / Fabric Clock

Differential interface, termination, integrated jitter and PLL transfer function.

Coherent Master

Stability, close-in phase noise, warm-up, aging, holdover and distribution.

Integration Boundary

Bare IC, module, evaluation board, sample-rate derivation and conditional RF / IF filtering.

Clock Interface

XTAL loop · CMOS · clipped sine · LVDS · LVPECL · HCSL · bias · termination.

Noise Translation

Reference multiplication · chirp linearity · detection floor · reciprocal mixing · spurs.

Sampling & Coherence

Jitter band · SNR / ENOB · SYSREF · phase alignment · deterministic latency.

Field Environment

Temperature · vibration · humidity · board bending · power integrity · lifecycle.

Architecture rule: never infer the reference clock from the radar carrier. Follow the actual device or board clock input, then qualify the crystal or oscillator against that node's electrical, spectral and environmental limits.

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Select by System Node First

Identify the replaceable clock function before comparing frequency, product class, electrical performance, qualification or package.

System Node	Clock Role	Representative Reference	Typical Device	Selection Focus
Bare Pulsed-Coherent Radar Sensor	External XIN / XOUT reference	24 MHz	Compact passive crystal	exact CL · ESR · C0 · drive · tolerance · startup · module boundary
Selected 60 GHz Radar MMIC	Device-specific oscillator loop	38.4 MHz	Passive crystal	exact device · loop interface · CL · ESR · drive · total ppm · startup
Automotive Radar SoC	Crystal or documented driven reference	40 / 50 MHz	AEC-Q200 crystal / qualified source	interface · ESR · load · drive · phase noise · -40 to +140°C mission profile
60 GHz FMCW Transceiver	Active chirp-PLL reference	76.8 / 80 MHz	Programmable CMOS XO	accuracy · RMS / peak jitter · duty cycle · startup · OE · amplitude
RFSoc / FPGA Fixed Board Clock	Clock-tree or device reference	100 MHz	Low-jitter differential XO	logic standard · termination · jitter band · PLL path · additive noise
RF Converter / Fabric Domain	ADC / DAC or fabric reference	122.88 / 125 MHz	Differential or CMOS XO by input	physical input vs sample rate · SYSREF · phase alignment · SNR / ENOB
High-Speed Serial / FPGA MGT	Transceiver reference	156.25 MHz	Low-jitter differential XO	AC coupling · common mode · termination · lane-rate mask · jitter
Coherent Instrument / Synthesizer	Disciplined master reference	10 MHz	TCXO / OCXO	phase noise · stability · warm-up · aging · holdover · load · distribution

1 · Identify the Function

Record whether the value is a passive loop, driven sensor reference, converter / MGT clock, coherent master, carrier, sample rate or filter center.

2 · Identify the Receiver / Circuit

Use the exact radar IC, MMIC, RFSoc, converter, FPGA, module or clock-device P/N together with its current schematic and clock tree.

3 · Apply Electrical / Spectral Limits

Define CL / ESR or waveform, phase noise, jitter, stability, synchronization, temperature and qualification before selecting a product.

Recommended sequence: platform documentation → physical node → integration boundary → exact frequency → interface → noise / stability budget → environment → qualification → final FCom configuration.

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Frequency & Component Placement Matrix

Each value is a selection anchor only after it has been mapped to the actual passive reference, driven clock, converter clock or coherent-master position.

Frequency / Range	Representative System Position	Applicability	Selection Interpretation
10 MHz	Disciplined source / synthesizer reference	Coherent Master	Select TCXO or OCXO by waveform, stability, phase-noise mask, warm-up, aging, holdover, power and distribution.
24 MHz	Bare pulsed-coherent-radar crystal loop	Acconeer A121 Example	A published example uses CL 9 pF and ESR 40 Ω. Confirm drive, C0, startup and the complete frequency-specific configuration.
38.4 MHz	Selected 60 GHz MMIC reference	Device-Specific Loop	Use a passive crystal only for the exact supported device and loop; do not substitute 40, 50, 76.8 or 80 MHz.
40 MHz	Automotive radar SoC reference	Automotive Review	TI AWR2544 supports 40 or 50 MHz options. Confirm crystal vs driven input, ESR, load, drive, phase noise and thermal mission.
50 MHz	Automotive radar SoC reference	Automotive Review	Public guidance includes ESR up to 50 Ω and operation to +140°C; final FCom series selection remains project-specific.
76.8 MHz	Driven CMOS FMCW reference	BGT60TR13C Option	Verify accuracy, RMS / peak jitter, startup, OE, duty cycle, edge rate, input amplitude and supply-noise sensitivity.
80 MHz	Driven CMOS FMCW reference	BGT60TR13C Typical	Compare jitter only using the platform's specified carrier, integration band, operating conditions and measurement method.
100 MHz	RFSoc / FPGA fixed differential clock	ZCU111 Board Clock	Confirm LVDS / LVPECL / HCSL interface, termination, jitter budget and whether a receiving PLL follows the source.
122.88 / 125 MHz	ADC / DAC, fabric or clock-tree reference	Converter / Fabric	Separate the physical board input from the converter sample rate; define SYSREF, phase alignment and jitter band.
156.25 MHz	FPGA high-speed serial / MGT reference	MGT Reference	Verify logic standard, AC coupling, common mode, termination, lane-rate mask and additive clock-tree jitter.

24 / 38.4 MHz

Passive sensor-reference positions for exact documented loops.

40 / 50 MHz

Automotive-radar nodes requiring full interface and thermal review.

76.8 / 80 MHz

Driven FMCW-reference inputs with explicit jitter conditions.

100-156.25 MHz

RF converter, fabric and MGT board-reference domains.

Reference interpretation: the carrier or converter sample rate is not automatically the external oscillator frequency. Select the physical component position shown by the current schematic and clock tree.

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Representative Platform & Architecture Matrix

Four public platforms illustrate bare-sensor, integrated FMCW, automotive-radar and direct-RF clock boundaries.

ACCONEER

A121 / XM125 / XE125 · 60 GHz Pulsed-Coherent Radar

1

Architecture: A121 integrates the 57–64 GHz RF front end, digitization, memory and antenna in package; XM125 adds an M4 MCU and module-level integration.

Public clock evidence: a bare A121 design uses a 24 MHz external crystal; the published example identifies CL 9 pF and ESR 40 Ω. The XM125 reference is integrated.

24 MHz Crystal → A121 60 GHz PCR → M4 / Host

Selection insight: FCX-1M can be reviewed for a bare A121 loop after exact CL, ESR, C0, drive and startup validation. An XM125-integrated reference is not presented as customer-replaceable.

INFINEON

DEMO-BGT60TR13C + Radar Baseboard MCU7

2

Architecture: the 58–63.5 GHz 1Tx / 3Rx antenna-in-package MMIC streams data through SPI to the radar baseboard and host tools.

Public clock evidence: Infineon guidance supports 76.8 or 80 MHz driven reference options and defines clock accuracy, jitter, startup, OE, duty-cycle and amplitude requirements.

76.8 / 80 MHz XO → BGT60TR13C → MCU7 / Host GUI

Selection insight: FCO-6P-PJ is an application-relevant CMOS starting family only after the exact supply, frequency and platform-defined jitter conditions are confirmed.

TEXAS INSTRUMENTS

AWR2544LOPEVM · 76–81 GHz Satellite Radar

3

Architecture: AWR2544 integrates a 4Tx / 4Rx radar front end, PLL, ADC, R5F and hardware accelerator, with Ethernet connectivity toward a central ECU.

Public clock evidence: the SoC supports 40 or 50 MHz crystal / driven reference options and publishes a –40 to +140°C operating profile.

40 / 50 MHz Ref → AWR2544 4Tx / 4Rx → Ethernet / ECU

Selection insight: the reference remains selectable, but no FCom series is assigned until crystal vs driven interface, frequency-specific ESR, qualification and the complete thermal mission are reviewed.

AMD

ZCU111 RFSoc + XM500 RFMC · Direct RF Sampling

4

Architecture: RF data-converter tiles connect to programmable logic and processing; LMK04208 and LMX2594 devices generate converter clocks and SYSREF.

Public clock evidence: fixed 100 / 125 MHz board clocks and a default 156.25 MHz MGT reference are separately documented from the internally generated sample clocks.

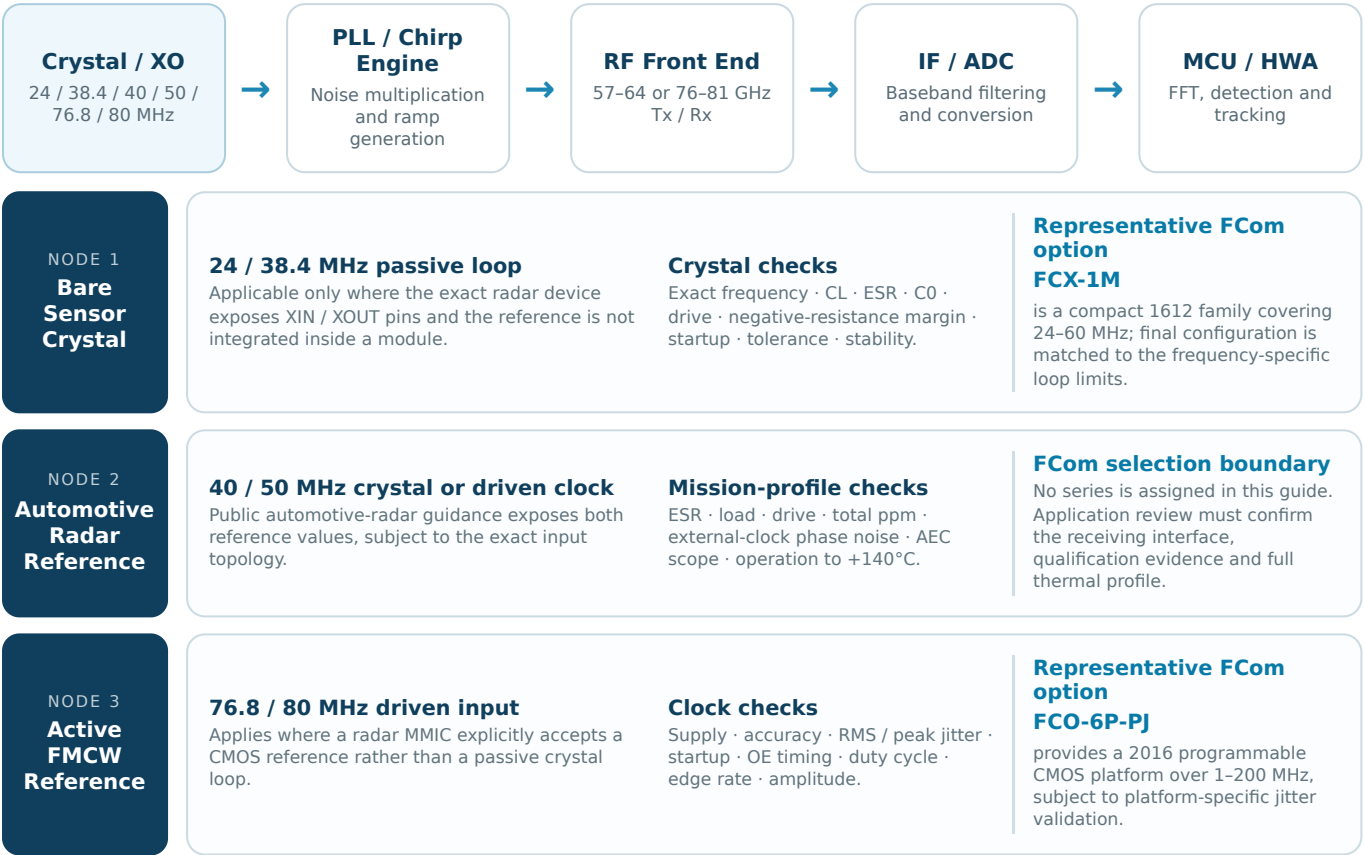
RF Front End → RFSoc ADC / DAC → PL / DSP / Network

Selection insight: FCO-2L-UJ is reviewed for a compatible fixed differential reference after output-standard, termination, phase-noise and integrated-jitter validation.

Platform interpretation: third-party names provide public architecture and clock-position context only. They do not indicate FCom adoption, approved-vendor-list status, qualification, compatibility or drop-in replacement.

05 Integrated Radar Sensor + FMCW Architecture

Representative placement of passive and driven reference functions in low-power 60 GHz and 76–81 GHz radar systems.

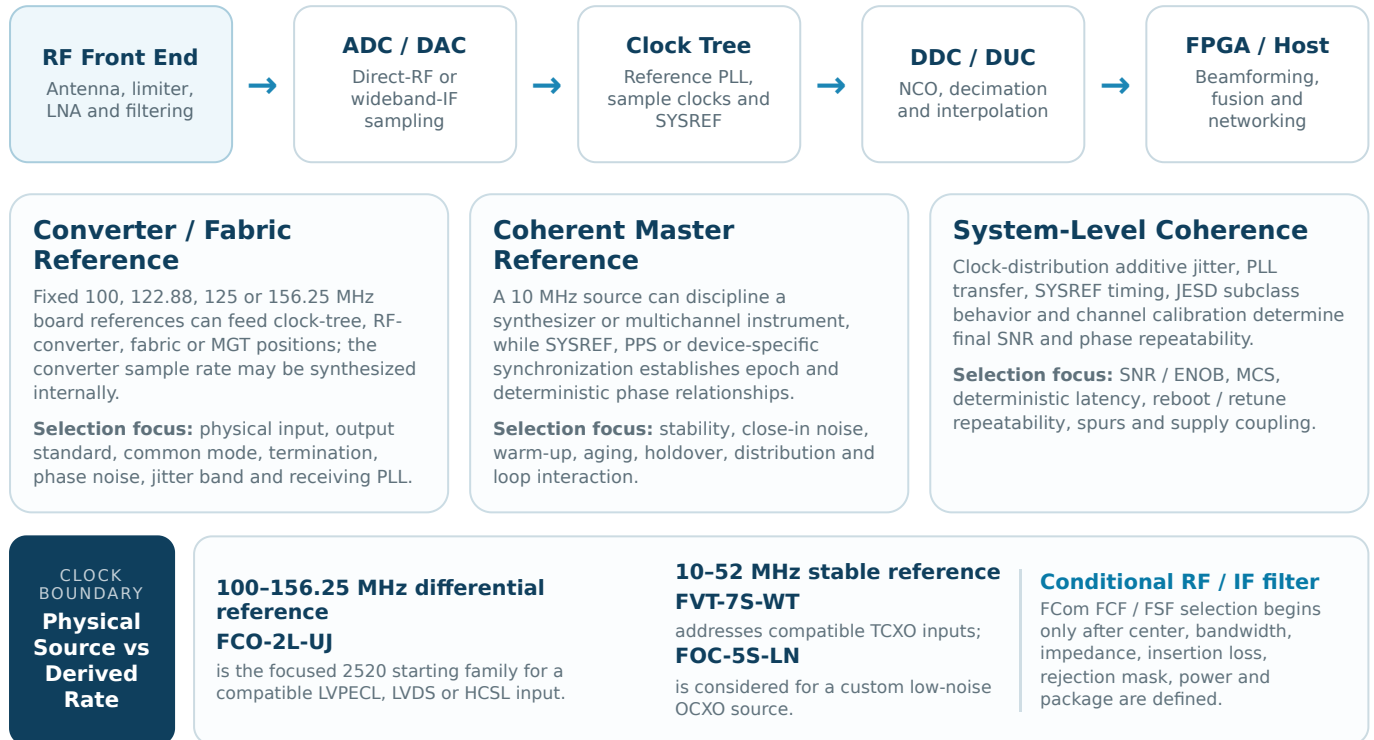


Architecture note: reference phase noise and spurs are multiplied through the radar PLL and can raise the detection floor or degrade chirp behavior. The lowest headline jitter value is not sufficient without the required integration band and offset mask.

06

Direct-RF Conversion + Coherent Sensing Architecture

Representative fixed-reference, converter-clock and synchronization decisions for RFSoc receivers, phased arrays and coherent instrumentation.



Architecture note: a sample-clock or RF-carrier value generated inside the PLL tree is not automatically a board-level oscillator requirement. FCom recommendations apply to documented, externally replaceable clock or filter positions.

07

FCom Selection Guidance by Design Condition

The options below correspond to defined, externally accessible radar-reference, converter-clock or coherent-master positions. Exact configurations follow circuit review.

Passive Sensor Reference

Compact crystal for an exposed, frequency-specific radar oscillator loop.

Active FMCW Clock

Programmable CMOS source for a documented 76.8 / 80 MHz input.

Converter Reference

Low-jitter differential oscillator for compatible 100–156.25 MHz nodes.

Stable / Coherent Master

TCXO or OCXO by stability, noise, warm-up and power budget.

Design Condition	FCom Selection	Representative Series / Portfolio Data	Key Check Before RFQ
24 / 38.4 MHz bare radar sensor exposes XTAL loop	FCX-1M	1612 4-SMD · 24–60 MHz · tolerance ± 5 ppm · stability ± 10 ppm · -40 to $+125^{\circ}\text{C}$ · CL 18 pF or specified · ESR 30–60 Ω by frequency.	Exact frequency · CL · ESR · C0 · drive · startup · module boundary
76.8 / 80 MHz radar MMIC accepts CMOS reference	FCO-6P-PJ	2016 4-SMD · 1–200 MHz · 1.8 / 2.5 / 3.3 V · CMOS · ± 15 ppm · -40 to $+125^{\circ}\text{C}$ · listed jitter 0.8 ps.	Jitter method / band · peak jitter · duty cycle · startup · OE · amplitude
100–156.25 MHz differential converter / MGT reference	FCO-2L-UJ	2520 6-SMD · 100–220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · ± 20 ppm · -40 to $+125^{\circ}\text{C}$ · listed jitter 50 fs.	Output standard · common mode · termination · jitter band · PLL path
10–52 MHz high-stability active reference	FVT-7S-WT	7050 4-SMD · 10–52 MHz · 2.5 / 3.3 V · best stability ± 50 ppb · -40 to $+105^{\circ}\text{C}$ · clipped sine / CMOS · pullability ± 5 ppm.	CLKIN support · waveform · tuning · phase noise · temperature · power
10 MHz low-noise coherent source	FOC-5S-LN	14 × 9 mm 6-SMD · 10–40 MHz · 3.3 / 5 V · best stability ± 50 ppb · -40 to $+85^{\circ}\text{C}$ · phase-noise references -120 / -145 / -157 / -162 dBc/Hz.	Output · load · warm-up · aging · holdover · power · distribution
40 / 50 MHz automotive radar reference	Project-specific review	No series assigned at guide level because the public device profile extends to $+140^{\circ}\text{C}$ and the passive / driven interface remains application-dependent.	AEC scope · interface · ESR / load / drive · phase noise · thermal mission
RF / IF path requires defined filtering	FCF / FSF after mask review	Crystal-filter or SAW-filter technology is selected only after the complete center, bandwidth, loss, rejection, impedance, power and package requirements are known.	Center · BW · loss · rejection · group delay · impedance · RF power

Application-specific boundary: series identifiers above are configurable FCom families, not complete orderable P/Ns. Final order codes follow frequency, supply, output, stability, temperature, load, package and qualification review.

ENGINEERING SELECTION SUPPORT

Request an FCom Radar Timing Review

Provide the target radar IC / module, physical clock or filter node, exact frequency, interface, noise / stability limits, temperature, qualification and project stage.

[Start Engineering Review →](#)

08

Engineering Validation & Minimum RFQ

Radar timing is defined by the physical node, oscillator interface, noise and stability budgets, synchronization method and operating environment.

Passive Radar Crystal

- Exact radar IC, oscillator pins and reference frequency
- CL, ESR, C0, drive and oscillation mode
- Negative-resistance margin and startup target
- Tolerance, stability, aging, package and AEC scope

Active FMCW / Board Clock

- Exact physical input and receiving-device P/N
- Waveform, amplitude / bias, common mode and termination
- VDD, current, duty cycle, startup, OE and warm-up
- Phase-noise mask and RMS / peak jitter definition

Converter / Coherence Requirements

- ADC / DAC input, SNR / ENOB and aperture-jitter budget
- SYSREF, JESD subclass and deterministic latency
- Clock-distribution additive jitter and phase alignment
- PLL transfer, channel repeatability and spur-sensitive zones

Environment, Filter & Program

- Temperature, vibration, humidity and board bending
- RF / IF center, passband, loss, impedance and rejection if required
- Automotive, industrial or laboratory qualification scope
- Samples, schedule, annual volume, lifecycle and change control

Minimum RFQ Information

Information Category	What to Provide
Application / Functional Node	Passive radar crystal, active FMCW reference, converter / MGT clock, coherent master or defined RF / IF filter position.
Target Device & Architecture	Exact radar IC, MMIC, RFSoc, converter, FPGA, module or clock-device P/N; schematic location, clock tree, reference BOM and revision.
Crystal / Clock Interface	CL / ESR / C0 / drive for a crystal loop, or waveform, level, bias, VDD, common mode, load, termination, enable and startup for an active source.
Noise & Stability	Phase-noise mask by offset, RMS / peak jitter definition and band, tolerance, temperature stability, aging, spurs and SNR / ENOB target.
Synchronization / RF Requirements	SYSREF, JESD subclass, phase alignment and repeatability; or RF / IF center, bandwidth, loss, rejection, impedance, power and matching.
Program Requirements	Operating environment, qualification / certification, validation plan, prototype quantity, sample date, annual volume and lifecycle.

Carrier Is Not the Reference

A 60 or 77 GHz carrier is synthesized from a lower clock. Select the physical crystal or driven input.

Jitter Must Be Defined

State carrier, integration band, output, load, supply and method before comparing headline values.

Module Boundaries Matter

An integrated module reference is not automatically customer-replaceable even when the bare sensor exposes one.

Frequency alone does not define the final part: the receiving interface, PLL transfer, noise / stability budget, synchronization method, environment and integration boundary determine the appropriate FCom series.

09

Engineering FAQ & Application Review

Common radar and RF-sensing timing questions, representative public references and the information required for FCom engineering review.

Is the radar carrier the oscillator frequency?

No. A 60 GHz or 76–81 GHz carrier is synthesized from a lower reference. Select from the radar IC's physical crystal or clock-input specification.

Can a crystal be replaced by a CMOS oscillator?

Only when the device supports a driven clock and its waveform, amplitude, duty cycle, startup and bias conditions are satisfied.

When is a specific FCom series shown?

Only when a public architecture exposes a replaceable node and the family has a relevant frequency, interface and performance envelope.

Why is no series named for 40 / 50 MHz automotive radar?

The public device profile extends to +140°C. Final selection therefore requires review of the interface, qualification evidence and vehicle thermal mission.

Can 50 fs and 0.8 ps jitter be compared directly?

Only with identical carrier, integration band, output, load, supply and measurement method. Request the phase-noise plot and jitter definition.

When should a TCXO or OCXO be used?

Use a TCXO for strong temperature stability with moderate power; use an OCXO for the strongest stability and close-in noise where warm-up is acceptable.

Why are no SAW filters assigned to the four platforms?

The public clock architectures do not expose a common replaceable IF filter mask. Selection requires center, bandwidth, impedance, loss and rejection.

Are the series identifiers complete orderable P/Ns?

No. The final suffix depends on frequency, supply, output, stability, temperature, load, package and qualification.

Representative Public Technical References

1. **Acconeer:** A121 Datasheet — 57–64 GHz sensor, 24 MHz crystal and oscillator-loop guidance.
2. **Acconeer:** XM125 / XE125 Documentation — module boundary and integrated sensor / host architecture.
3. **Infineon:** DEMO-BGT60TR13C — 58–63.5 GHz 1Tx / 3Rx FMCW evaluation platform.
4. **Infineon:** 60 GHz MMIC schematic guidance — device-specific reference-clock options.
5. **Texas Instruments:** AWR2544 Datasheet — 76–81 GHz 4Tx / 4Rx radar SoC and 40 / 50 MHz references.
6. **Texas Instruments:** AWR2544LOPEVM — satellite-radar evaluation architecture.
7. **AMD:** ZCU111 RF Data-Converter Clocking — reference PLL, RF PLL, converter clocks and SYSREF.
8. **AMD:** ZCU111 Clock Generation — fixed 100 / 125 / 156.25 MHz board-reference domains.

FCom product specification note: configurable product information in this guide is presented at series or representative-configuration level. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation.

ENGINEERING REVIEW

Radar & RF Sensing Timing Review

Provide the target radar IC / module, replaceable clock or filter node, exact frequency, interface, noise / stability limits, synchronization needs, temperature, package, qualification and project stage. FCom can recommend the most relevant configuration for system validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Third-party names are used solely as public technical references. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by complete board- and system-level validation.