

PROFESSIONAL RADIO, SDR & RF/IF SIGNAL PROCESSING

Professional Radio, SDR & RF/IF Signal Processing

Coordinate frequency references, converter clocks and IF / RF selectivity across professional radio, digital-IF, software-defined-radio and direct RF-sampling platforms.

Reference Integrity + IF Selectivity + Low-Jitter Sampling + Multichannel Coherence

Mission-Critical Radio

Land Mobile Radio

Digital IF

Software-Defined Radio

Direct RF Sampling

Test & Instrumentation

Application Scope

Conventional superheterodyne radios, narrow and wideband digital-IF receivers, integrated RF transceivers, coherent SDR arrays, RFSOC platforms and precision radio test equipment.

Selection Philosophy

Selection begins with the physical, replaceable function. A carrier, LO, IF center, sample rate, FPGA clock and external reference may coexist in one system but are not interchangeable component positions.

System Reference

10 MHz disciplined source and synchronization boundary for coherent systems.

Radio Reference

Exact-frequency crystal or active clock for the RF transceiver or IF subsystem.

Converter Clock

Low-jitter differential source for ADC, DAC, JESD and FPGA clock trees.

IF / RF Selectivity

Crystal or SAW filtering defined by bandwidth, loss, rejection and impedance.

01

Application Scope & Engineering Domains

Professional-radio and SDR platforms combine reference, sampling and signal-selectivity functions that require different component classes and validation criteria.

Separate the reference, signal and sampling domains. A radio may expose a 10 MHz synchronization input, a 26 or 38.4 MHz device reference, a 10.7–450 MHz IF path and a 100–500 MHz converter clock. Each value belongs to a different physical node.

Typical Equipment

Professional & Mission-Critical Radio

Land-mobile radio
Public-safety terminals
Base and repeater stations
Secure telemetry
Channelized receivers

SDR & Digital IF

Agile transceivers
Digital-IF receivers
Coherent radio arrays
Spectrum monitoring
Software-defined gateways

RF Sampling & Instrumentation

RFSoc platforms
Direct-sampling radios
Wideband data conversion
Signal analyzers
Laboratory radio systems

Five Engineering Domains

Reference & Synchronization

10 MHz, PPS, phase alignment, warm-up, aging and holdover.

Device Reference

Passive loop or driven input at the exact transceiver / IF-subsystem frequency.

Converter & Fabric Clock

Logic interface, integrated jitter, additive noise and deterministic timing.

IF / RF Selectivity

Passband, ripple, loss, rejection, group delay, impedance and RF power.

Integration Boundary

Bare IC, evaluation board, module and externally selectable host functions.

Clock Interface

XTAL loop · clipped sine · CMOS · LVDS · LVPECL · HCSSL · bias · termination.

Noise Budget

Phase noise by offset · RMS jitter band · reciprocal mixing · SNR / ENOB · spurs.

Filter Mask

Center · occupied BW · poles · ripple · insertion loss · rejection zones · matching.

Coherence & Environment

MCS / MTS · PPS · retune / reboot repeatability · temperature · shock · lifecycle.

Architecture rule: do not map an RF carrier, LO setting, IF center, sample rate or FPGA master-clock rate directly to a timing product until the current schematic confirms a physical crystal, oscillator or external-clock input at that node.

02

Select by System Node First

Identify the replaceable clock or filter function before comparing frequency, product class, electrical performance or package.

System Node	Clock / Signal Role	Representative Frequency	Typical Device	Selection Focus
External System Reference	Frequency discipline / coherent synchronization	10 MHz	OCXO / disciplined source	waveform · amplitude · impedance · phase noise · warm-up · aging · holdover
IF-Subsystem Reference	On-chip LO and clock synthesizers	26 MHz	XO / TCXO or crystal by interface	FREF topology · exact level · synthesizer plan · close-in noise · startup
Integrated RF-Transceiver Reference	RF PLL / device-clock domain	38.4 MHz	VCTCXO / TCXO or crystal	clock input vs loop · tuning · phase noise · stability · multichip sync
Narrow First / Second IF	Channel selectivity before demodulation	10.7 / 21.4 / 38.855 / 45 MHz	Crystal filter	3 dB BW · poles · ripple · loss · rejection · termination · group delay
Wideband Analog / Digital IF	ADC input and channel-conditioning path	70-450 MHz	SAW / crystal filter by mask	occupied BW · stopband zones · impedance · matching · RF power
ADC / DAC / JESD Clock Tree	Converter and FPGA reference	100-220 MHz	Low-jitter differential XO	logic standard · common mode · termination · jitter band · additive noise
High-Rate / Pullable Clock	Converter, fabric or clock-cleaner input	245.76-500 MHz class	Programmable XO / VCXO	supported rate · phase-noise mask · pull range · loop BW · deterministic phase
Frequency-Specific IF / RF Path	Narrow IF or receiver preselection	110 / 450 MHz	Fixed SAW filter	passband · insertion loss · rejection · impedance · power · layout

1 · Identify the Function

Record whether the value is a crystal loop, driven reference, converter clock, crystal IF, SAW IF / RF path, carrier, LO or internally generated rate.

2 · Identify the Receiver / Circuit

Use the exact transceiver, ADC / DAC, RFSoc, FPGA, module or clock-device P/N together with its schematic pins and clock tree.

3 · Apply Electrical / Spectral Limits

Define interface, phase noise, jitter, stability or the complete filter mask, impedance and RF-power requirements before selecting a product.

Recommended sequence: platform documentation → physical node → circuit interface → exact frequency → noise or filter budget → synchronization → environment → package → final FCom configuration.

03

Frequency & Component Placement Matrix

Each value is a selection anchor only after it has been mapped to the actual reference, converter-clock or IF / RF-filter position.

Frequency / Range	Representative System Position	Applicability	Selection Interpretation
10 MHz	External reference / disciplined system source	Common System Reference	Confirm waveform, level, impedance, phase-noise mask, warm-up, aging and holdover before considering an OCXO-based source.
26 MHz	IF-subsystem FREF or on-board reference	AD9864 / AD9874 Example	Use an active source only at a documented clock input; a passive loop requires separate crystal-loop review.
38.4 MHz	Integrated RF-transceiver reference	ADRV9002 Example	Verify clock-input topology, tuning requirement, phase noise, temperature stability and multichip-sync configuration.
10.7 MHz	Narrow first / second IF filter	Crystal IF Position	FCF-9T / FCF-9U Type 10M7.5B is a starting point only when bandwidth, poles, termination, loss and group delay match.
21.4 / 38.855 / 45 MHz	Channelized first or second IF selectivity	Frequency-Specific IF	Select the exact FCF series + Type from the channel mask; center frequency alone does not establish compatibility.
70-450 MHz	Wideband analog IF into a converter	Digital-IF Range	Confirm whether the design needs narrow channel filtering or a wider RF / IF passband before choosing FCF or FSF technology.
110 MHz	Frequency-specific digital-IF filter	Fixed SAW IF	FSF4090-110M-1M152-4-40 is relevant only when its 1.152 MHz BW, loss, rejection and impedance fit the path.
100-220 MHz	ADC / DAC / FPGA differential clock	Low-Jitter Clock	Confirm LVPECL / LVDS / HCSL interface and the application-specific phase-noise or integrated-jitter requirement.
245.76-500 MHz	Converter, fabric or clock-cleaner input	High-Rate Clock	Distinguish a physical board input from an internally generated sample or master rate; add VCXO pullability only when a control loop requires it.
1.0 / 1.28 / 2.0 GHz	Selected RFSoc master / converter rate	Platform-Generated Rate	A platform rate may be synthesized internally. FCO-3L-PG is listed to 1.5 GHz; 2 GHz is outside that series range.

10 / 26 / 38.4 MHz

System and radio-reference positions with different interfaces.

10.7-450 MHz

Crystal or SAW IF / RF paths defined by the complete filter mask.

100-500 MHz

Common low-jitter converter, JESD and FPGA clock domains.

1-2 GHz Rates

Platform master or converter rates that may be internally synthesized.

Reference interpretation: carrier, LO, IF, sample-clock, MCR and external-reference values are separate domains. Select the physical component position shown by the current schematic and clock tree.

04

Representative Platform & Architecture Matrix

Four public platforms illustrate narrow digital IF, integrated agile SDR, wideband digital IF and direct RF-sampling selection boundaries.

ANALOG DEVICES

EVAL-AD9864 / EVAL-AD9874 · Narrow Digital IF

1

Architecture: a low-level 10–300 MHz IF is conditioned and digitized for decimation and serial I/Q processing.

Public clock evidence: ADI documents an external FREF option or an on-board 26 MHz XO for the on-chip LO and clock synthesizers; signal bandwidth spans 6.8–270 kHz.

RF Tuner / Mixer → Crystal / SAW IF → AD9864 / AD9874

Selection insight: evaluate FVT-6S only for a compatible driven 26 MHz FREF. Select the FCF / FSF position separately against the actual IF channel mask.

ANALOG DEVICES + AMD / XILINX

EVAL-ADRV9002 + ZCU102 / ZC706 · Agile SDR

2

Architecture: the 2 × 2 direct-conversion transceiver covers 30 MHz–6 GHz with 12 kHz–40 MHz transmit / receive bandwidth.

Public clock evidence: the evaluation flow uses a 38.4 MHz VCTCXO by default, within a broader documented device-clock and multichip-synchronization architecture.

FEM / Antenna → ADRV9002 → Zynq FPGA / CPU

Selection insight: FVT-6S is the compact starting family for a compatible active reference; consider FVT-7S-HP only when its stability and temperature class improve the verified system budget.

ANALOG DEVICES + AMD / XILINX

EVAL-AD6676 + ZC706 · Wideband Digital IF

3

Architecture: the AD6676 digitizes a 70–450 MHz IF with 20–160 MHz bandwidth and transfers data over JESD204B.

Public clock evidence: ADI's board flow uses a 200 MHz clock by default, with 125 / 150 / 250 MHz alternatives; published configurations also show internally generated converter rates.

70–450 MHz IF → AD6676 Σ-Δ ADC → JESD204B / ZC706

Selection insight: FCO-3L-UJ is the focused 200 MHz differential-clock starting family. FCO-3L-PG covers a compatible 250 MHz physical clock position after interface and jitter review.

NI / ETTUS RESEARCH

USRP X440 · Direct RF-Sampling Platform

4

Architecture: a balun-only RF path feeds RFSoc ADC / DAC resources, followed by NCO, DDC / DUC and RFNoC processing.

Public clock evidence: the manual documents validated master-clock examples from 125 MHz to 2 GHz, dual-rate operation and a 10 MHz / PPS synchronization boundary.

FBX Balun → RFSoc ADC / DAC → RFNoC / QSFP

Selection insight: FOC-5S-LN can support a customer-designed external 10 MHz reference source. The X440 MCR values remain internal platform rates, not automatic oscillator selections.

Platform interpretation: these public examples provide architecture and frequency context only. They do not indicate FCom adoption, qualification, compatibility or drop-in replacement. Final selection follows the latest datasheet, schematic, BOM, clock configuration, errata and operating profile.

05 Conventional Radio + Narrow / Digital IF Architecture

Representative placement of radio-reference, crystal / SAW IF and converter-clock functions in a channelized professional receiver.

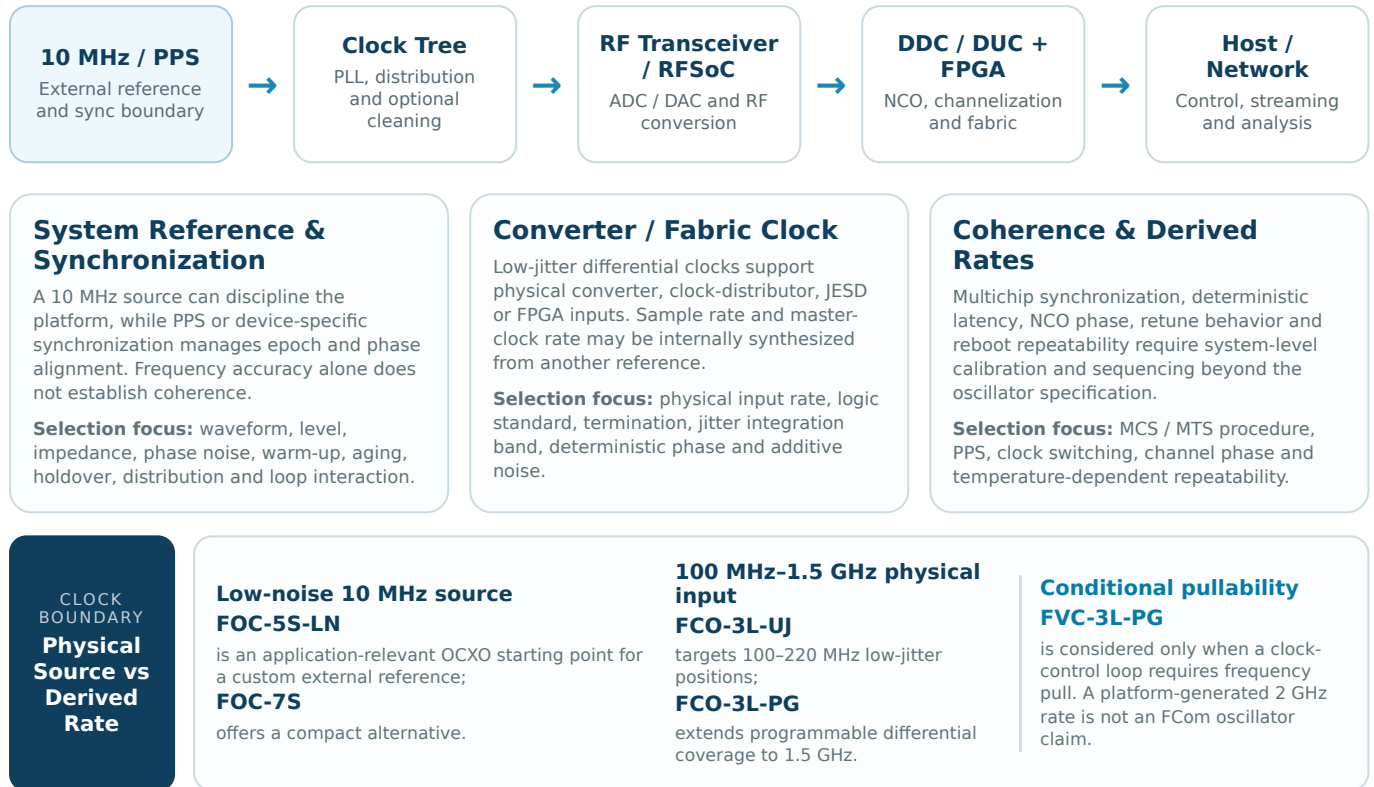


Architecture note: reference noise can be multiplied by synthesizers and appear as reciprocal mixing, EVM degradation or converter SNR loss. Validate phase noise at the relevant offsets and RMS jitter over a stated integration band.

06

Integrated SDR + Direct RF-Sampling Architecture

Representative reference, converter-clock and synchronization decisions for agile transceivers, RFSoc radios and coherent multi-channel systems.



Architecture note: evaluation-board oscillator locations and platform MCR values do not automatically remain customer-selectable in the final design. FCom recommendations apply only to documented physical clock inputs or externally replaceable reference-source circuits.

07

FCom Selection Guidance by Design Condition

The options below correspond to defined, externally accessible reference, converter-clock or IF / RF-filter positions. Exact configurations follow circuit review.

System Reference

Low-noise or compact OCXO for a defined 10 MHz source design.

Radio Reference

Passive crystal or compatible TCXO / VCTCXO by receiving interface.

Converter Clock

Low-jitter, programmable or pullable differential source by clock-tree need.

IF / RF Function

Crystal filter series + Type or complete frequency-specific SAW P/N.

Design Condition	FCom Selection	Representative Series / Portfolio Data	Key Check Before RFQ
Custom 10 MHz low-noise reference source	FOC-5S-LN / FOC-7S	10-40 MHz OCXO families · best listed stability ± 5 ppb; FOC-5S-LN phase-noise references $-120 / -145 / -157 / -162$ dBc/Hz at 10 Hz / 100 Hz / 1 kHz / 10 kHz.	Output · level · impedance · warm-up · aging · holdover · package
26 / 38.4 MHz device accepts active reference	FVT-6S / FVT-7S-HP	FVT-6S: 2016 · 10-52 MHz · 1.8-3.3 V · clipped sine · best stability ± 0.5 ppm · -40 to $+85^\circ\text{C}$. FVT-7S-HP: 7050 · best listed stability ± 50 ppb · up to $+105^\circ\text{C}$.	CLKIN support · level / bias · tuning · stability · phase noise
Radio IC exposes a passive crystal loop	FCX-2S	Application-specific crystal starting family; final configuration is matched to the exact frequency and oscillator-loop electrical limits.	Exact frequency · CL · ESR · C0 · drive · mode · startup
100-220 MHz low-jitter differential clock	FCO-3L-UJ	3225 6-SMD · 100-220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · ± 20 ppm · -40 to $+125^\circ\text{C}$ · listed jitter 50 fs.	Output standard · amplitude · termination · jitter band · phase noise
High-rate fixed programmable source	FCO-3L-PG	3225 6-SMD · 10-1500 MHz · 2.5 / 3.3 V · LVPECL / LVDS · stability ± 25 ppm · -40 to $+105^\circ\text{C}$ · listed jitter 0.6 ps.	Physical input rate · phase-noise mask · harmonic plan · load
Clock-control loop requires pullability	FVC-3L-PG	3225 6-SMD · 10-1500 MHz · 2.5 / 3.3 V · LVPECL / LVDS · stability ± 25 to ± 50 ppm · pullability ± 50 to ± 150 ppm.	Control voltage · pull range · loop bandwidth · modulation sensitivity
Narrow IF or fixed 110 / 450 MHz path	FCF series + Type / FSF fixed P/Ns	FCF: 10M7.5B, 21MQ75A, 38.8M15B and 45MQ75A. FSF: FSF4090-110M-1M152-4-40 and FSF3838-450M-4M-2-50 .	Center · BW · poles · loss · rejection · group delay · impedance · RF power

Application-specific boundary: a passive crystal, active TCXO / VCTCXO, fixed XO, pullable VCXO, crystal IF filter and SAW filter address different circuit functions. They are not interchangeable without receiving-interface and signal-path validation.

ENGINEERING SELECTION SUPPORT

Request an FCom Radio Timing & IF / RF Review

Provide the target platform, physical clock or filter node, exact frequency, interface, noise / filter limits, synchronization needs, environment, package and project stage.

[Start Engineering Review →](#)

08

Engineering Validation & Minimum RFQ

Professional-radio selection is defined by the physical node, circuit interface, noise or filter budget, synchronization method and operating environment.

Reference / Active Clock

- Exact device P/N and physical reference position
- Frequency, waveform / bias, VDD, load and termination
- Phase-noise, jitter, stability, startup and warm-up limits
- Pull range and control loop only where required

Passive Crystal Loop

- Exact receiving IC, oscillator pins and frequency
- CL, ESR, C0, drive and oscillation mode
- Negative-resistance margin and startup target
- Tolerance, stability, aging, layout and stray capacitance

IF / RF Filter Position

- Center, occupied bandwidth and channel plan
- Insertion loss / ripple and rejection by frequency zone
- Poles, group delay, impedance, matching and S-parameters
- RF power, blockers, harmonics and front-end topology

Synchronization, Environment & Program

- PPS, MCS / MTS, deterministic latency and phase repeatability
- Temperature, shock, vibration, humidity and power integrity
- Qualification, EMC / radio certification and change control
- Samples, schedule, annual volume and lifecycle

Minimum RFQ Information

Information Category	What to Provide
Application / Functional Node	10 MHz system reference, 26 / 38.4 MHz radio reference, passive crystal loop, converter / FPGA clock, crystal IF or SAW IF / RF position.
Target Device & Architecture	Exact transceiver, ADC / DAC, RFSoC, FPGA, module or clock-device P/N; schematic location, clock-tree diagram, reference BOM and revision.
Clock / Oscillator Interface	CL / ESR / C0 / drive for a crystal loop, or waveform, level, bias, VDD, load, enable, startup, warm-up and pullability for a driven source.
Noise & Stability	Phase-noise mask by offset, RMS jitter limit and integration band, tolerance, temperature stability, aging, spurs, SNR / ENOB or reciprocal-mixing target.
IF / RF Requirements	Center, occupied BW, passband / ripple, insertion loss, stopband zones, group delay, impedance, matching, S-parameters, power and blockers.
Program Requirements	Operating environment, qualification / certification, validation plan, prototype quantity, sample date, annual volume, production location and lifecycle.

Rate Is Not Always a Source

Carrier, LO, sample and MCR values may be synthesized internally. Confirm the physical clock input before selecting an oscillator.

Noise Must Be Band-Limited

State phase-noise offsets and the RMS jitter integration range. A family-level jitter value does not guarantee converter SNR.

Center Frequency Is Not a Filter

Bandwidth, poles, ripple, loss, rejection, termination, group delay and power define the usable IF / RF component.

Frequency alone does not define the final part: the receiving interface, clock tree, noise or filter budget, synchronization method, environment and integration boundary determine the appropriate FCom series or frequency-specific P/N.

09

Engineering FAQ & Application Review

Common professional-radio, SDR and RF / IF questions, representative public references and the information required for FCom engineering review.

Are carrier, LO, IF, sample-clock and reference frequencies interchangeable?

No. They are separate circuit domains. Select from the physical crystal, oscillator, clock-input or filter position shown by the current schematic.

Can a 38.4 MHz reference replace 26 MHz?

No. Use the exact frequency and interface required by the transceiver or IF subsystem. Software settings do not make unlike references drop-in compatible.

When should a 10 MHz reference use an OCXO?

When phase-noise, aging, temperature, warm-up or holdover budgets justify it. Waveform, level, impedance and the disciplining loop must also match.

Does a listed 50 fs oscillator guarantee converter SNR?

No. Final SNR depends on actual frequency, jitter integration band, additive clock-tree noise, signal frequency, power integrity and PCB implementation.

Can FCO-3L-PG provide every RFSoc master-clock rate?

No. The series is listed to 1.5 GHz, and many MCR values are generated inside the platform. Confirm the external physical input before selection.

When is a VCXO preferable to a fixed XO?

When a control loop requires frequency pull for cleaning, discipline or synchronization. Without that loop, a fixed low-jitter source is normally clearer.

Can a crystal IF filter be replaced by a SAW filter at the same center?

Not by frequency alone. Bandwidth, shape factor, loss, group delay, termination, rejection and power behavior determine compatibility.

Why are some FCom entries series names and others complete P/Ns?

Configurable timing products require a final order code. The listed FSF filters are complete frequency-specific P/Ns; FCF filters use series + Type.

Representative Public Technical References

- Analog Devices:** EVAL-AD9864 / AD9874 — IF range, bandwidth, external FREF and 26 MHz board reference.
- Analog Devices:** AD9864 product and datasheet — IF subsystem, synthesizer and digital-output architecture.
- Analog Devices:** ADRV9002 product and datasheet — 2 × 2 agile-transceiver architecture and operating range.
- Analog Devices:** ADRV9002 system-level guide — evaluation clocking, interfaces and synchronization.
- Analog Devices:** AD6676 product and datasheet — 70-450 MHz IF and wideband digital-IF architecture.
- Analog Devices:** AD6676-EBZ project — 200 MHz default and 125 / 150 / 250 MHz board-clock context.
- NI / Ettus:** USRP X4x0 manual — X440 signal path, validated MCR families and synchronization boundary.
- NI / Ettus:** X440 sampling-rate and master-clock-rate guidance.

FCom product specification note: configurable product information in this guide is presented at series or representative-configuration level. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation.

ENGINEERING REVIEW

Professional Radio, SDR & RF/IF Signal Processing Review

Provide the target platform, replaceable clock or filter node, exact frequency, interface, noise / stability or filter-mask requirements, synchronization needs, environment, package and project stage. FCom can recommend the most relevant configuration for system validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Third-party names are used solely as public technical references. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by complete board- and signal-path validation.