

PLC & INDUSTRIAL CONTROLLERS

PLC & Industrial Controllers

Coordinate processor, Industrial Ethernet and retained-time clock domains for reliable control, communication and event logging across PLC and industrial-controller platforms.

Processor Timing + Real-Time Control + Industrial Ethernet + Communication + Retained-Time

Compact & Modular PLC

Remote I/O

Industrial Controller

EtherCAT / PROFINET

EtherNet/IP / TSN

RTC / Event Logging

Application Scope

PLC CPUs, industrial MCUs / MPUs, real-time controllers, remote I/O, Industrial Ethernet modules, communication gateways and controllers requiring retained-time / event logging.

Selection Philosophy

Selection begins with the receiving clock node. Processor, Industrial Ethernet, high-speed network and RTC references form separate timing domains even when they coexist within the same controller.

Processor

MCU / MPU / FPGA main reference and PLL input.

Real-Time Control

Deterministic control, I/O and communication processing.

Industrial Ethernet

PHY, EtherCAT controller, switch and gateway timing.

Retained-Time

RTC, event timestamp, fault and maintenance logging.

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Application Scope & Engineering Domains

PLC platforms combine deterministic processing, industrial networking and retained-time functions, each with a different external clock role.

One controller, multiple timing domains. The PLC CPU, EtherCAT / Ethernet subsystem, communication controller and RTC may each use a different reference source. Timing selection therefore begins with the receiving IC and its documented clock input.

Typical Equipment

PLC & Control

Compact PLC
Modular PLC
Safety PLC
Machine Controller
Process Controller

Distributed Control

Remote I/O
Edge Controller
Communication Module
Industrial Gateway
Industrial PC Controller

Industrial Networking

EtherCAT
PROFINET
EtherNet/IP
Modbus TCP
TSN / Gigabit Ethernet

Five Engineering Domains

Processor & Controller

MCU / MPU / FPGA main clock and PLL reference.

Real-Time Control & I/O

Deterministic control, timers, I/O and FPGA timing.

Industrial Ethernet

PHY / ESC / switch / network processor reference.

Industrial Communication

CAN, RS-485, USB and fieldbus-controller timing.

RTC & Event Logging

Retained-time, power-loss and fault-history reference.

Oscillator Interface

XTAL pins · CMOS CLKIN · differential REFCLK · external RTC clock.

Frequency Accuracy

Relevant to processor startup, Ethernet tolerance and retained-time accuracy.

Jitter / SI

Becomes a first-order parameter in FPGA, Gigabit Ethernet and SerDes reference paths.

Industrial Environment

Operating temperature, EMI / EMC, lifecycle and system validation.

Clock-definition note: CPU operating frequency, PLC scan cycle, PWM frequency, ADC sample rate, encoder pulse rate, EtherCAT cycle time, CAN bit rate and Ethernet line rate are internal or interface-domain values and are distinct from the external crystal or oscillator reference.

02

Select by System Node First

Begin with the receiving clock input, then determine frequency, device class, performance requirements and package.

System Node	Clock Role	Representative External Reference	Typical Device	Selection Focus
PLC CPU / Industrial MCU	Main processor / PLL reference	20 / 24 MHz 12 / 16 / 40 / 48 MHz platform-dependent	Crystal / CMOS XO	XTAL vs CLKIN · CL / ESR · startup · ppm · temperature
Real-Time Controller / FPGA	Logic / fabric reference	25 / 50 / 100 MHz class	CMOS / low-jitter XO	jitter · logic level · load · system topology
Industrial Ethernet PHY	PHY reference	25 MHz	Crystal / XO	CL · ESR · drive level · accuracy · shared clocking
EtherCAT / ESC	Protocol-controller reference	25 MHz common platform-specific alternatives	Crystal / XO	ESC requirements · PHY clock distribution
RMII Interface	Driven interface reference	50 MHz	CMOS clock / forwarded clock	source direction · clock sharing · receiver CLKIN
Gigabit Ethernet / Switch	MAC / switch / high-speed reference	125 MHz	CMOS / differential XO	architecture · jitter · output logic
High-Speed FPGA / SerDes	High-speed REFCLK	100 / 125 / 156.25 MHz	Low-jitter differential XO	LVDS / LVPECL / HCSL · jitter · termination
RTC / Event Logging	Retained-time reference	32.768 kHz	Tuning-fork crystal / kHz XO	XTAL vs driven CLKIN · CL · ESR · current

1 · Identify the Receiver

Identify the PLC processor, PHY, ESC, switch, FPGA or RTC device together with the clock pins used in the design.

2 · Classify the Clock Domain

Evaluate processor, Industrial Ethernet, high-speed network and retained-time references as distinct timing domains before comparing timing devices.

3 · Apply Electrical Constraints

Define CL / ESR for crystals, or VDD / output / jitter for driven clocks, together with the required temperature range and package.

Recommended sequence: System node → clock input type → frequency → crystal / XO class → accuracy / jitter → temperature → package → final FCom configuration.

03

Frequency & Component Placement Matrix

Frequency becomes meaningful when it is considered together with the receiving node and the clock architecture used by the controller.

Frequency	Representative System Position	Applicability	Selection Interpretation
32.768 kHz	RTC / retained-time / event logging	Common Retained-Time Reference	External tuning-fork crystal or low-current driven clock depending on RTC topology.
10 / 12 / 16 MHz	MCU / communication controller	Platform-Dependent	The selected MCU oscillator interface defines the reference requirement; scan time and communication bit rate remain separate system parameters.
20 MHz	Real-time MCU / control processor	Control-Platform Reference	Typical external reference for selected real-time MCU platforms, with higher CPU clocks synthesized internally.
24 MHz	PLC CPU / industrial MPU	Common Processor Reference	Frequently used as an external processor PLL reference in industrial MCU / MPU platforms.
25 MHz	Ethernet PHY / EtherCAT / Industrial Ethernet	Common External Reference	A core Industrial Ethernet timing anchor; crystal, XO and shared-clock architectures are evaluated according to the target PHY / ESC interface.
40 / 48 MHz	MCU / USB / communication controller	Interface-Dependent	Used by selected controller and interface architectures.
50 MHz	RMII / driven Ethernet reference	Often Forwarded / Driven	May be generated by a PHY from a 25 MHz source or supplied by an external XO, depending on the RMII clock topology.
100 MHz	FPGA / PCIe / high-speed logic	High-Speed Extension	Driven reference where jitter and clock-interface type become important.
125 MHz	Gigabit Ethernet / MAC / switch	High-Speed Network Reference	Can be an external oscillator or part of a forwarded / distributed clock tree.
156.25 MHz	High-speed Ethernet / SerDes / FPGA	High-Speed Extension	Typically a low-jitter driven reference; output logic and jitter integration band are key.

20 / 24 MHz
 Processor / real-time control anchor frequencies.

25 MHz
 Primary Industrial Ethernet / EtherCAT external reference.

125 / 156.25 MHz
 Gigabit / FPGA high-speed reference layer.

32.768 kHz
 Retained-time and event-logging clock domain.

Reference-clock interpretation: 100 Mbps / 1 Gbps Ethernet, EtherCAT cycle time, PLC scan time, PWM frequency and CPU operating frequency do not directly define the crystal / oscillator frequency. The external reference is taken from the receiving IC clock specification.

04

Representative Platform & Architecture Matrix

Four public platforms illustrate real-time PLC processing, EtherCAT clock distribution, dedicated Industrial Ethernet processing and multi-clock retained-time architecture.

TEXAS INSTRUMENTS

TMDS243EVM / AM243x · Real-Time PLC & Industrial Communications

1

Architecture: Arm Cortex-R5F real-time processing combined with PRU-ICSSG industrial communication subsystems, Ethernet, time synchronization and control-oriented peripherals.

Public evidence: the platform supports industrial Ethernet, standard Ethernet, PCIe and FSI; AM243x supports EtherCAT, PROFINET, EtherNet/IP, IO-Link and TSN.

Real-Time CPU → PRU-ICSSG → Industrial Ethernet

Selection insight: processor operating clocks, deterministic control timing and Industrial Ethernet synchronization form distinct timing domains within the same control platform.

BECKHOFF

ET1100 · EtherCAT Slave Controller & 25 MHz Clock Distribution

2

Architecture: 25 MHz crystal or oscillator feeds the EtherCAT Slave Controller; when a crystal is used, ET1100 can provide 25 MHz CLK25OUT to Ethernet PHYs.

Public evidence: Beckhoff specifies 25 MHz OSC_IN with initial accuracy of 25 ppm or better and publishes crystal / oscillator clock-sharing examples.

25 MHz XTAL / XO → ET1100 ESC → PHY Clock

Selection insight: a single 25 MHz source can support multiple network devices, while crystal and oscillator architectures lead to different distribution and loading considerations.

RENESAS

YCONNECT-IT-RZN2L · Industrial Ethernet / TSN Network Processor

3

Architecture: host application MCU connects to RZ/N2L through a host interface; the network processor integrates Industrial Ethernet functionality and dual Gigabit PHY connections.

Public evidence: the kit supports EtherCAT, EtherNet/IP and Modbus and is prepared for TSN-based real-time Ethernet using Gigabit PHYs.

Host PLC MCU → RZ/N2L → Gigabit PHYs

Selection insight: host-controller timing and Industrial Ethernet timing may reside in separate clock domains and should be evaluated independently.

MICROCHIP

SAM9X75 · Multi-Clock Industrial Controller Architecture

4

Architecture: processor, Gigabit Ethernet and slow-clock domains coexist on one industrial MPU platform.

Public clock evidence: Microchip publishes 24 MHz for the processor main clock, 25 MHz and 125 MHz for Ethernet clock generation, plus 32.768 kHz for the slow / retained-time domain.

24 MHz Processor → 25 / 125 MHz Ethernet → 32.768 kHz RTC

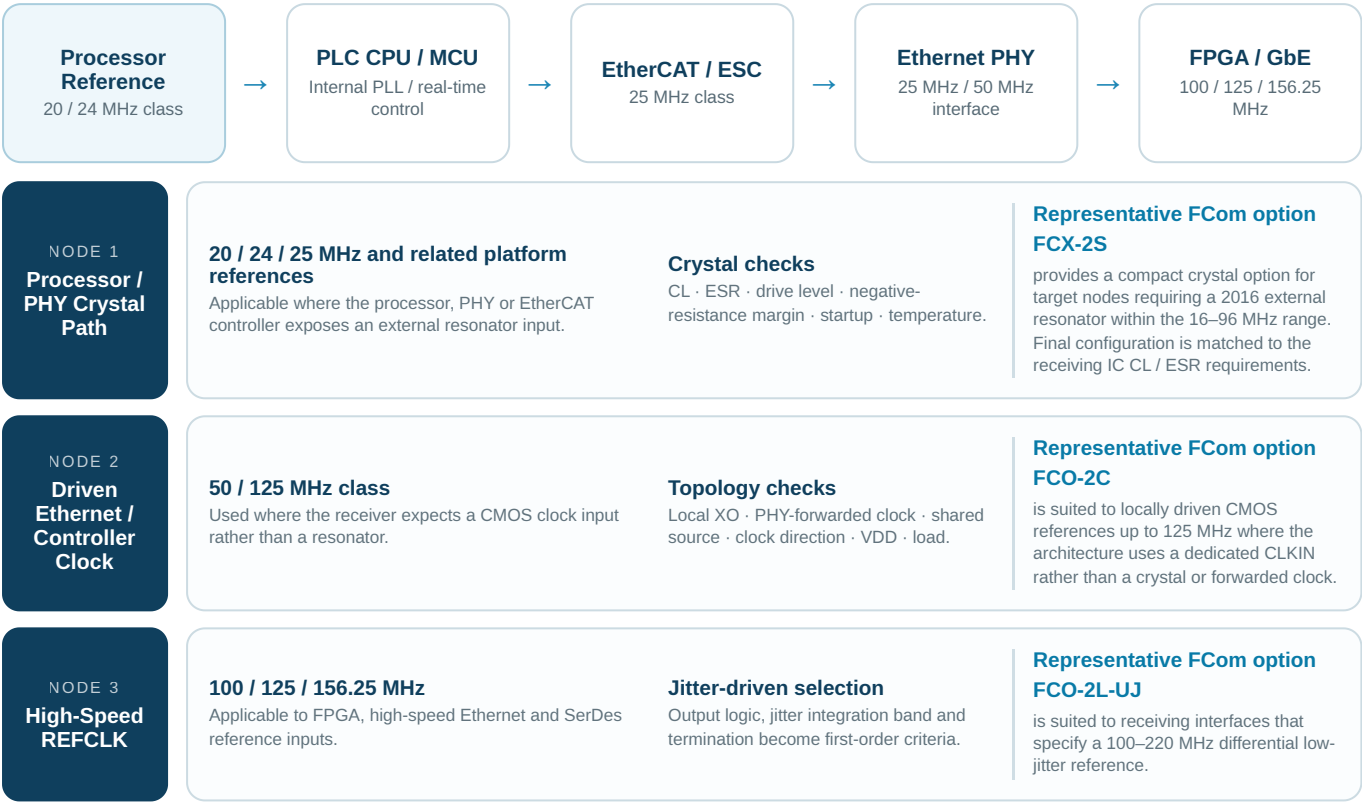
Selection insight: one controller can require several timing-device classes; the system node and clock interface determine the appropriate component class.

Platform interpretation: these public examples are provided to illustrate representative timing architectures. They do not indicate FCom adoption, qualification, compatibility or drop-in replacement. Final selection is based on the exact target-device documentation, schematic and complete system requirements.

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PLC CPU + Industrial Ethernet Timing Architecture

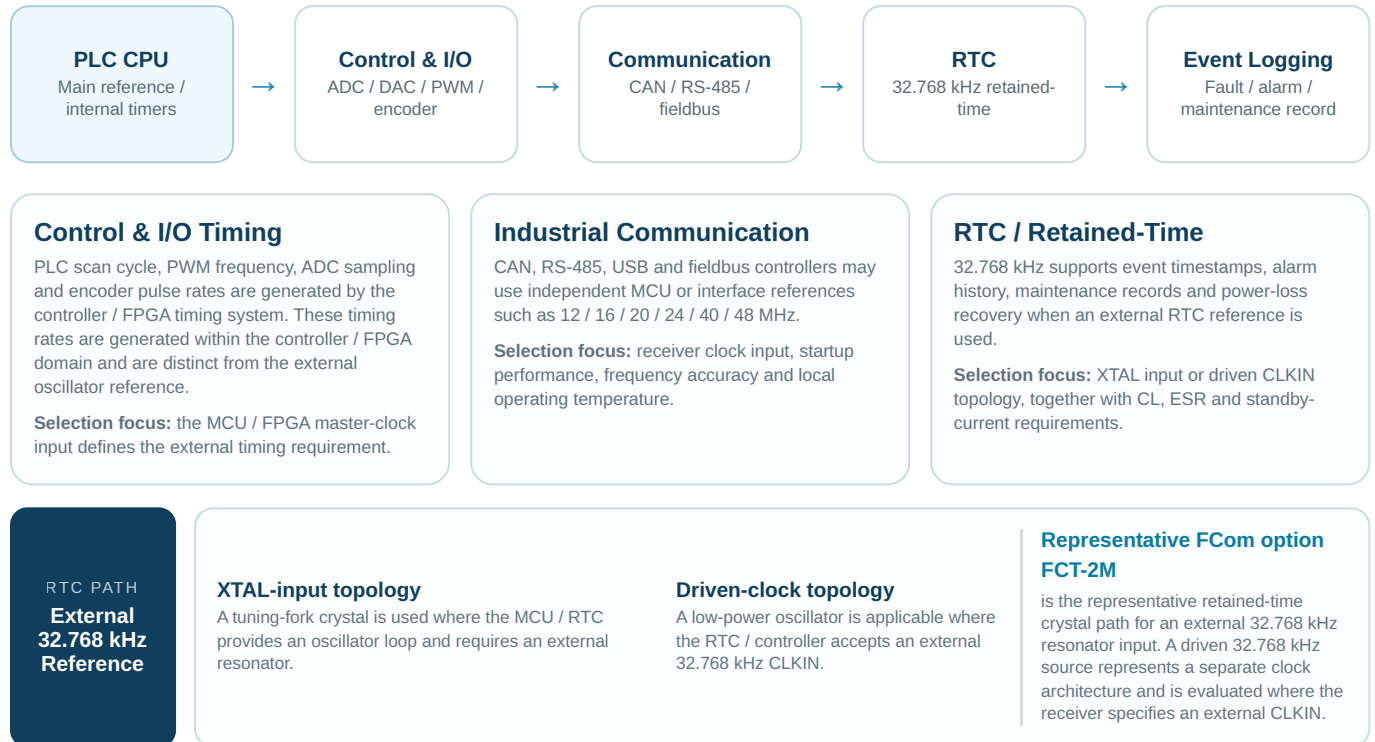
Representative external timing from the PLC processor into EtherCAT / Ethernet and high-speed network nodes.



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Control + Communication + Retained-Time Architecture

Representative timing around PLC control logic, field communication and RTC / event-logging functions.



Architecture note: retained-time is an independent clock domain. A PLC can use its main processor reference for normal operation while the RTC / timestamp domain remains active through low-power or backup-power states.

07 FCom Selection Guidance by Design Condition

The product families below correspond to the primary timing decisions in PLC and industrial-controller architectures. Exact ordering codes are confirmed after the receiving clock interface is defined.

Processor / PHY XTAL
 External resonator input in the 16–96 MHz class.

Driven CMOS Clock
 Local 50 / 125 MHz-class reference when the node expects CLKIN.

Low-Jitter Differential
 100 / 125 / 156.25 MHz high-speed network REFCLK.

Retained-Time
 32.768 kHz external crystal for RTC / event logging.

Design Condition	FCom Selection	Why It Changes the Decision	Key Check Before RFQ
Processor / PHY exposes XTAL pins	FCX-2S	The crystal path applies where the receiving IC provides an oscillator loop and requires an external resonator.	Frequency · CL · ESR · startup margin · package
Receiver expects local driven CMOS CLKIN	FCO-2C	Applicable where the clock node uses a locally driven source instead of a crystal or forwarded reference.	Frequency · VDD · logic threshold · load · OE
100–220 MHz + differential + explicit low jitter	FCO-2L-UJ	Applicable to high-speed Ethernet / FPGA / SerDes interfaces where output logic and RMS jitter define the device class.	LVDS / LVPECL / HCSL · jitter band · termination · VDD
RTC exposes 32.768 kHz XTAL pins	FCT-2M	Dedicated retained-time crystal path for RTC, event logging and low-power timestamp functions.	RTC topology · CL · ESR · backup-power behavior

Application-specific extensions: low-power driven 32.768 kHz clocks, wider-temperature CMOS XO, low-CL crystals, programmable / spread-spectrum clocks, TCXO / OCXO and tunable VCXO / VCTCXO can be evaluated when the system introduces specific requirements for driven RTC CLKIN, –55°C operation, very-low CL, EMI management, precision synchronization, holdover or frequency tuning. Crystal Filter and SAW products address separate communication / RF filtering functions and therefore sit outside the core PLC clock-selection path.

ENGINEERING SELECTION SUPPORT

Request an FCom PLC Timing Recommendation

Provide the target processor / PHY / ESC / FPGA / RTC part number, clock pins, frequency, CL / ESR or supply / output, jitter requirement, temperature, package and project stage.

[Start Engineering Review →](#)

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Engineering Validation & Minimum RFQ

PLC timing is defined by the receiving node, clock topology and system environment in addition to frequency.

Processor / MCU / FPGA

- Exact IC part number
- XTAL or CLKIN interface
- Frequency
- CL / ESR or VDD / logic
- Startup / jitter if specified
- Operating temperature

Industrial Ethernet

- PHY / ESC / switch P/N
- EtherCAT / PROFINET / EtherNet/IP / TSN
- 25 / 50 / 125 MHz clock topology
- Crystal, local XO or shared clock
- Accuracy / jitter / termination requirements

Control & Communication

- Control MCU / FPGA / interface P/N
- CAN / RS-485 / USB / fieldbus architecture
- Master-clock input
- Isolation / EMI environment
- Package and lifecycle constraints

RTC / Event Logging

- MCU / RTC P/N
- XTAL pins or external CLKIN
- 32.768 kHz CL / ESR or VDD / current
- Backup-power architecture
- Timestamp / retained-time objective

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	PLC CPU, real-time MCU, FPGA, EtherCAT controller, Ethernet PHY / switch, communication controller or RTC.
Target Device	Exact receiving IC part number and clock pin / schematic location.
Clock Topology	External resonator, local CMOS XO, shared / forwarded clock, differential REFCLK or external 32.768 kHz source.
Crystal Requirements	Frequency, package, CL, ESR, tolerance / stability, drive level and operating temperature.
XO Requirements	Frequency, VDD, output logic, stability, temperature, RMS jitter / integration band, load, OE and termination.
Program Requirements	Prototype quantity, sample date, validation plan, annual volume, production location, lifecycle and compliance documentation.

25 MHz Can Use Different Topologies

A 25 MHz node may be a processor crystal, Ethernet PHY crystal, EtherCAT ESC reference or shared oscillator output.

50 MHz RMII Is a Clock-Topology Decision

RMII REF_CLK can be generated by a PHY or supplied externally; the clock direction and source architecture are defined by the PHY / controller topology.

32.768 kHz Supports Two External Paths

RTC may use a tuning-fork crystal oscillator loop or accept a low-power driven clock input.

Frequency alone does not define the final part: the receiving device, clock-interface type and network / RTC topology determine the appropriate FCom series and exact electrical configuration.

09

Engineering FAQ & Application Review

Common PLC timing questions, representative public architecture references and the information required for FCom engineering review.

Is the PLC CPU operating frequency the external crystal frequency?

No. The external reference feeds the oscillator / PLL domain; higher processor clocks are normally generated internally.

Does EtherCAT cycle time determine the crystal frequency?

No. EtherCAT cycle time is a network / control timing parameter. The ESC and PHY use their own documented external references.

Why is 25 MHz important in Industrial Ethernet?

Many Ethernet PHY and EtherCAT-controller architectures use a 25 MHz crystal or oscillator reference, sometimes with shared clock distribution to PHYs.

Does every Ethernet PHY need a separate crystal?

No. Depending on the PHY / ESC design, clocks can be shared, generated or forwarded from another device.

When is a low-jitter differential XO appropriate?

It is appropriate when FPGA, Gigabit Ethernet or SerDes receivers specify a differential REFCLK with a defined RMS-jitter limit.

What is 32.768 kHz used for in a PLC?

It supports retained-time functions such as fault / alarm timestamps, event logs, maintenance history and time retention through low-power states.

Does 1 Gbps Ethernet imply a 1 GHz oscillator?

No. Ethernet line rate and the external reference clock are different parts of the PHY / MAC timing architecture.

When are TCXO / OCXO solutions relevant?

They are application-specific options for systems that define tighter synchronization, holdover or reference-accuracy requirements than a standard crystal / XO path.

Representative Public Technical References

1. **Texas Instruments:** TMDS243EVM — AM243x evaluation platform with industrial Ethernet, standard Ethernet, PCIe and FSI.
2. **Texas Instruments:** AM2434 — real-time MCU architecture supporting EtherCAT, PROFINET, EtherNet/IP, IO-Link and TSN.
3. **Beckhoff:** ET1100 Hardware Description — 25 MHz crystal / oscillator reference and CLK25OUT clock-distribution examples.
4. **Renesas:** YCONNECT-IT-RZN2L — Industrial Ethernet SoM with EtherCAT, EtherNet/IP, Modbus and Gigabit PHYs.
5. **Renesas:** RZ/N2L — TSN-compliant 3-port Gigabit Ethernet switch and Industrial Ethernet processor.
6. **Microchip:** SAM9X75 industrial MPU / SOM clock architecture — 24 MHz processor, 25 / 125 MHz Ethernet and 32.768 kHz slow-clock references.

FCom product specification note: product information in this guide is presented at series or representative-configuration level. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

PLC & Industrial Controller Timing Review

Provide the target processor / FPGA / EtherCAT / PHY / switch / RTC part number, clock input, frequency, CL / ESR or supply / output, jitter target, operating temperature, package and project stage. FCom can review the requirement and recommend an appropriate timing series and configuration for system validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.