

PCS, GAMING & CONSUMER COMPUTING

PCs, Gaming & Consumer Computing

This guide helps designers coordinate processor-platform references, low-jitter PCIe and high-speed interface clocks, USB and Ethernet timing, display and wireless references, and peripheral timing across consumer-computing systems.

Compute + PCIe + USB + Ethernet + Display + Wireless + Peripheral Control

Notebook PCs

Mini PCs

Consumer PCs

Game Consoles

Handheld Gaming

Controllers & Accessories

Application Scope

CPU / SoC and GPU platforms, PCIe expansion, USB hubs and docks, Ethernet PHYs, display bridges, wireless controllers, audio and peripheral-control domains.

Selection Philosophy

Selection begins with the receiving clock node.
External reference frequency, oscillator topology, output logic and jitter limits remain independent of CPU frequency, interface generation and data rate.

Compute

Processor fixed references, platform timing and local controller clocks.

High-Speed I/O

PCIe, FPGA, SerDes and expansion-interface reference clocks.

Connectivity

USB, Ethernet, Wi-Fi, Bluetooth and docking-station timing.

Peripherals

Display bridges, embedded controllers, gaming accessories and RTC domains.

01

Application Scope & Engineering Domains

Consumer-computing platforms combine fixed processor references, interface-specific clock trees and peripheral oscillator loops that must be evaluated as separate timing domains.

Notebook / Mini PC

A processor platform connects PCIe storage and expansion, USB-C, display, Ethernet, wireless modules and embedded controllers through multiple clock domains.

Console / Handheld

A high-performance SoC combines graphics, display, storage, networking, USB and low-latency peripheral interfaces within a thermally constrained platform.

Controller / Accessory

Wireless SoCs, sensors, haptics, audio and always-on control may use compact MHz and 32.768 kHz oscillator loops independently of the host system.

Processor Platform

Fixed crystal references and internal PLLs establish the base timing used by compute and integrated I/O functions.

PCIe / Expansion

100 MHz differential REFCLK, SSC topology and interface-generation limits govern storage, GPU and expansion timing.

USB / Ethernet / Display

Hubs, PHYs and bridges may expose local 24, 25 MHz or platform-specific reference inputs.

Wireless / Always-On

Wireless SoCs and controllers commonly separate the radio HFXO from a 32.768 kHz sleep or RTC domain.

Platform Fixed

38.4 MHz class



PCIe

100 MHz differential REFCLK



USB / Ethernet

24 MHz; 25 MHz → derived 125 MHz



Display / Wireless

12 / 19.2 / 26 / 27 / 32 / 40 / 48 MHz class



Accessory RTC

32.768 kHz where exposed

Reference Frequency

Use the external XTAL or CLKIN requirement of the receiving device, not processor operating frequency, display refresh rate or interface throughput.

Clock Quality

Jitter must be tied to output logic, integration band, receiver mask, SSC mode and complete signal-integrity environment.

Clock Ownership

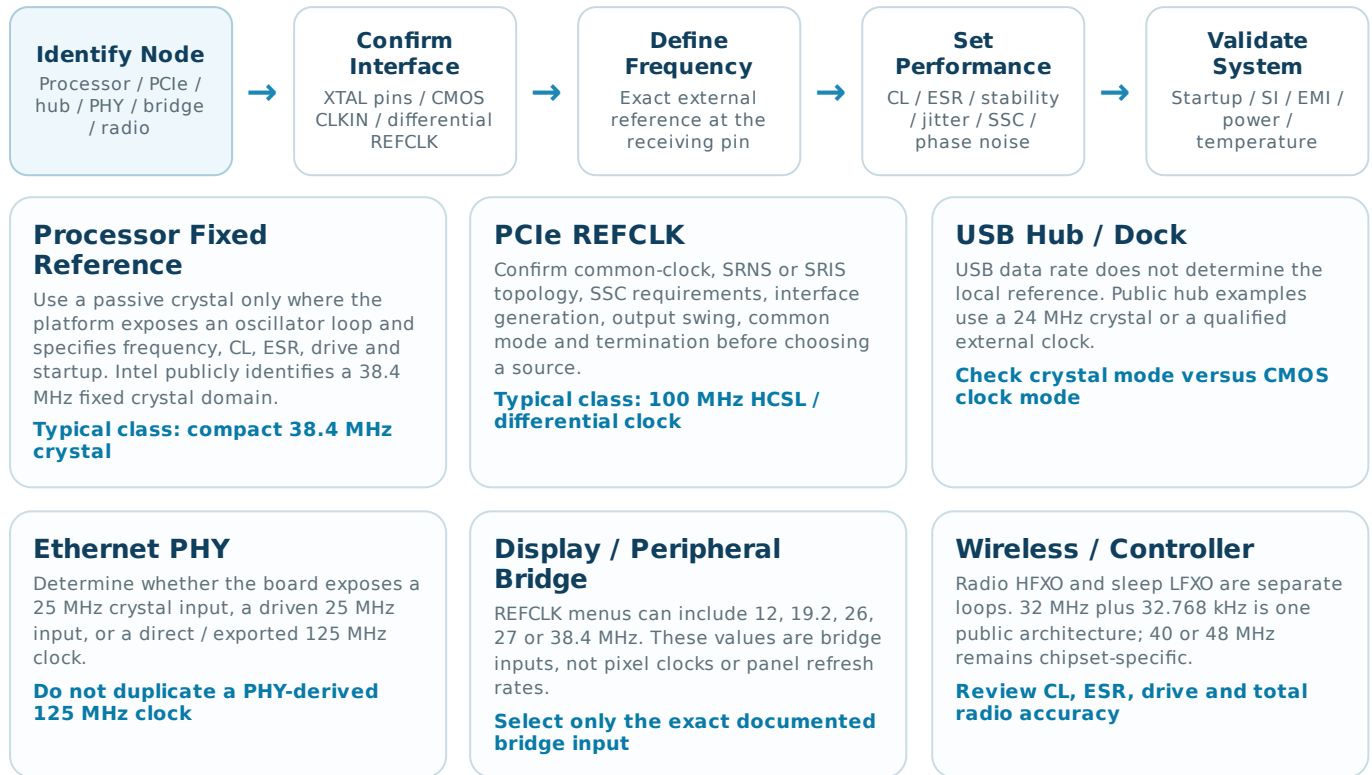
A module, PHY or platform clock generator may already derive the required clock. Confirm the boundary before adding a local oscillator.

System-rate boundary: CPU/GPU GHz, DDR data rate, PCIe GT/s, USB Gb/s, Ethernet line rate and display refresh do not directly specify the external crystal or oscillator frequency.

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Select by System Node First

Identify the receiving IC and clock interface before selecting passive-crystal or driven-clock topology, exact frequency, output format and performance class.



Topology rule: a passive crystal, CMOS XO and differential XO are not interchangeable merely because they share a nominal frequency. The receiving circuit defines the component class.

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Frequency & Component Placement Matrix

The frequency families below are architecture checkpoints. Final values remain controlled by the exact receiving device, clock-input mode and schematic.

Frequency / Band	Representative System Node	Device Class	Selection Boundary
32.768 kHz	Controller RTC, embedded controller, sleep / wake domain	Conditional Timebase	Use a tuning-fork crystal for XTAL pins or a low-current XO only for a documented driven CLKIN.
12 / 19.2 / 26 / 27 / 38.4 MHz	Selected display bridge or peripheral reference input	Platform-Specific REFCLK	Values may be alternatives within one bridge family. They are not universal PC clocks.
24 MHz	USB hub, display controller, peripheral controller	Common Peripheral Reference	Confirm passive-crystal versus driven-clock mode and the receiver's CL, ESR, startup and jitter limits.
25 MHz	Gigabit Ethernet PHY or clock-generator input	Common PHY Input	May be multiplied internally to 125 MHz or used to generate other system clocks.
32 / 40 / 48 MHz	Wireless SoC, controller, connectivity subsystem	Radio / Controller HFXO	Exact value, load and accuracy are controlled by the selected chipset and radio mode.
38.4 MHz	Processor fixed reference and selected bridge domains	Node-Specific Fixed Clock	The same frequency may serve unrelated receivers; validate each oscillator loop independently.
100 MHz	PCIe storage, GPU, FPGA and expansion reference	Differential Low-Jitter REFCLK	Confirm HCSL / LVDS / LVPECL, SSC topology, termination and the PCIe receiver mask.
125 / 156.25 MHz	Conditional Ethernet, 10GbE, FPGA or high-speed network expansion	Architecture-Dependent Clock	125 MHz may be PHY-derived; 156.25 MHz is not a default consumer-PC reference.

Platform

38.4 MHz fixed reference where the processor architecture exposes it.

Peripheral

24 / 25 MHz hub, PHY, controller or generator input.

High-Speed

100 MHz PCIe; conditional 125 / 156.25 MHz network clocks.

Wireless

32 / 40 / 48 MHz radio HFXO and conditional 32.768 kHz LFXO.

Frequency Match

Confirm the exact external reference instead of using a nearby bridge, radio or interface value.

Electrical Match

Passive CL / ESR and active VDD / logic / load / OE requirements must match the receiving node.

Performance Match

PCIe jitter, radio accuracy, Ethernet clock direction and controller startup are different specifications.

Interpretation: a frequency appearing in several subsystems does not make the devices interchangeable. The receiving pin, topology and validation limits remain the source of truth.

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Representative Platform & Architecture Matrix

Four public architectures show where external timing components enter compute, USB, Ethernet and wireless-accessory clock trees.

INTEL

Core Ultra · Meteor Lake U/H Platform

1

Architecture: processor platform with PCIe, Display, Time Stamp Counter and USB Type-C clock domains.

Public timing evidence: 38.4 MHz fixed clock without SSC supplies Display, SVID, TSC and USB Type-C; 100 MHz PCIe reference with SSC supplies PCIe controllers.

38.4 MHz Fixed → Processor Domains ← 100 MHz PCIe

FCom selection point: FCX-1S / FCX-2S are representative compact-crystal families for evaluation after oscillator-loop review. FCO-2L-UJ may be evaluated only when the 100 MHz input, output format and SSC topology are satisfied.

TEXAS INSTRUMENTS

TUSB8041EVM · Four-Port USB 3.0 Hub

2

Architecture: one upstream host connection feeds four downstream SuperSpeed / USB 2.0 ports through the TUSB8041 hub controller.

Public timing evidence: 24 MHz fundamental crystal, CL 12-24 pF, stability ± 100 ppm or better and ESR $\leq 50 \Omega$; external-clock mode has explicit peak-to-peak jitter limits.

24 MHz XTAL / CLK → TUSB8041 → 4 × USB Ports

FCom selection point: An exact 24 MHz FCX-2S configuration may be evaluated only if it meets the $\leq 50 \Omega$ ESR requirement. FCO-1C may be evaluated only for the documented driven-clock mode and after review against the complete jitter limits.

TEXAS INSTRUMENTS

DP83867ERGZ-R-EVM · Gigabit Ethernet PHY

3

Architecture: host MAC connects through RGMII to a 1000/100/10BASE PHY and the copper Ethernet interface.

Public timing evidence: the EVM uses an onboard 25 MHz crystal and can provide a 125 MHz reference clock derived from that crystal; IEEE 1588 SFD timestamping is supported.

25 MHz Crystal → DP83867 PHY → Derived 125 MHz

FCom selection point: FCX-2S is a representative passive-crystal family for evaluation. A direct 125 MHz FCO-3P-UJ or differential source should be considered only when the selected MAC/PHY mode exposes that input.

NORDIC SEMICONDUCTOR

nRF5340 / nRF7002 DK · Wireless Accessory

4

Architecture: wireless host SoC separates the radio high-frequency oscillator from RTC, sleep and wake timing.

Public timing evidence: 32 MHz HFXO plus optional 32.768 kHz LFXO. The LFXO improves low-frequency accuracy; the DK populates it by default and requires it for ANT / ANT+.

32 MHz HFXO → Wireless SoC ← 32.768 kHz LFXO

FCom selection point: FCX-2S and FCT-1S provide representative FCom starting points for the two oscillator-loop classes. Final CL, C0, ESR, drive and radio-accuracy limits must be confirmed from the selected SoC design.

Platform-use boundary: third-party platforms illustrate clock-insertion points only. They do not imply FCom adoption, qualification, endorsement, verified compatibility or drop-in replacement.

Compute

38.4 MHz fixed and 100 MHz PCIe are separate domains.

USB

24 MHz crystal and driven-clock modes require different checks.

Ethernet

25 MHz may generate the board's 125 MHz clock internally.

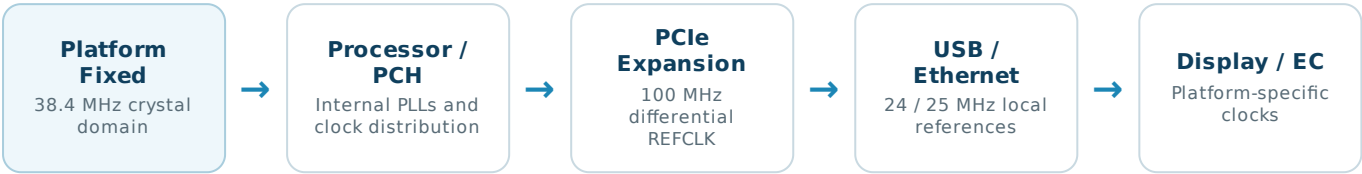
Wireless

32 MHz radio timing remains separate from 32.768 kHz sleep timing.

05

Notebook / Mini PC Timing Architecture

Representative component placement from the processor fixed reference through PCIe expansion, USB / Ethernet peripherals and display or controller clocks.



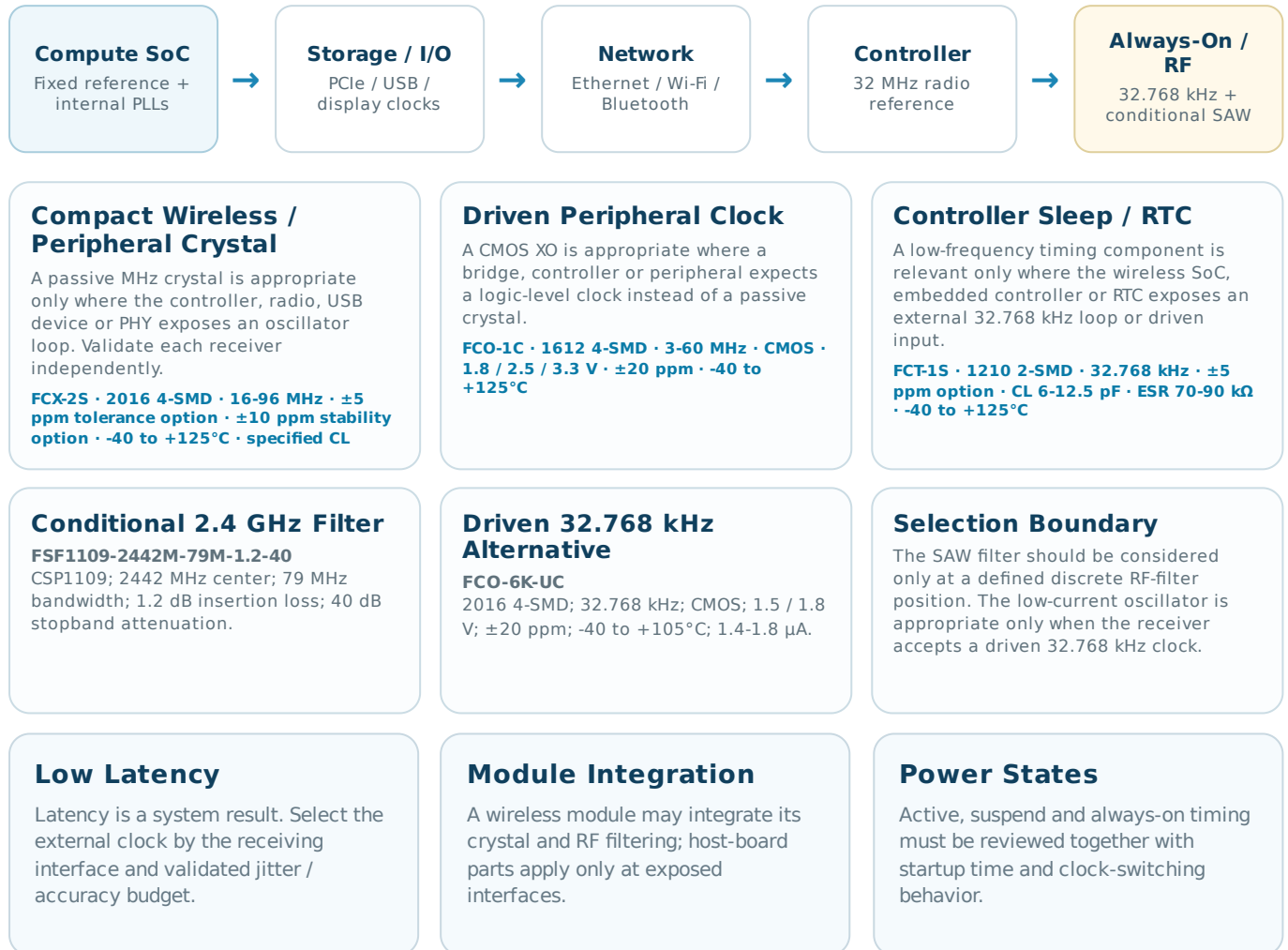
NODE 1 38.4 MHz Fixed Reference	Processor oscillator loop A compact passive crystal may be considered only where the processor platform exposes and documents a fixed crystal interface.	Selection checks CL · ESR · drive · startup · tolerance / stability · temperature · PCB parasitics.	Representative FCom option FCX-1S — 1210 4-SMD; 24-76.8 MHz; tolerance options down to ±5 ppm; stability options down to ±10 ppm; -40 to +125°C; specified CL; ESR 60-100 Ω by frequency. Final 38.4 MHz configuration requires platform-loop validation.
NODE 2 100 MHz PCIe REFCLK	Differential high-speed clock A local source may be used only where the root complex, endpoint or clock tree specifies a 100 MHz differential input.	Interface checks HCSL / LVDS / LVPECL · PCIe topology · SSC · swing · common mode · termination · receiver mask.	Representative FCom option FCO-2L-UJ — 2520 6-SMD; 100-220 MHz; 1.8 / 2.5 / 3.3 V; LVPECL / LVDS / HCSL; ±20 ppm; -40 to +125°C; 50 fs reference phase-jitter value. Confirm guaranteed limit, integration band, PCIe compliance and SSC implementation.
NODE 3 24 / 25 MHz Peripheral Reference	USB hub / Ethernet PHY Local passive references may be exposed by a hub, dock controller, PHY or platform clock generator.	Receiver checks Exact frequency · CL · ESR · drive · ppm budget · startup; verify whether 125 MHz is internally derived.	Representative FCom option FCX-2S — 2016 4-SMD; 16-96 MHz; tolerance options down to ±5 ppm; stability options down to ±10 ppm; -40 to +125°C; specified CL; ESR 30-100 Ω by frequency. Select an exact 24 / 25 MHz configuration against the receiver limit.

Architecture note: the 38.4 MHz processor fixed reference, 100 MHz PCIe REFCLK and 24 / 25 MHz peripheral references are separate nodes. One valid frequency or component class must not be copied automatically across them.

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Gaming Console, Handheld & Accessory Architecture

Representative timing around a performance SoC, high-speed expansion, local connectivity, wireless controllers and retained-time domains.



Architecture note: wireless reference, RTC timing and RF filtering are different component decisions. A 2.4 GHz SAW filter is not a timing device and is not a default element of every gaming controller or accessory.

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FCom Selection Guidance by Design Condition

The selections below are limited to positions where the target architecture creates a clear component decision. Exact ordering configurations are confirmed after the receiving interface is defined.

Miniature XTAL

Processor, hub, PHY, bridge or wireless oscillator loop.

Driven CMOS

Peripheral, controller or bridge with a documented CLKIN.

Low-Jitter Differential

PCIe / FPGA / high-speed receiver with an explicit clock mask.

Conditional RF / RTC

Discrete 2.4 GHz filter or external 32.768 kHz timing position.

Design Condition	FCom Selection	Series-Level Specifications	Key Check Before RFQ
24-76.8 MHz + smallest passive footprint	FCX-1S	1210 4-SMD; ± 5 ppm tolerance option; ± 10 ppm stability option; -40 to +125°C; specified CL; ESR 60-100 Ω by frequency.	Exact frequency · CL · ESR · drive · startup
16-96 MHz + broader passive-loop coverage	FCX-2S	2016 4-SMD; ± 5 ppm tolerance option; ± 10 ppm stability option; -40 to +125°C; specified CL; ESR 30-100 Ω by frequency.	Receiver ESR limit · negative resistance · PCB parasitics
3-60 MHz driven peripheral clock	FCO-1C	1612 4-SMD; CMOS; 1.8 / 2.5 / 3.3 V; ± 20 ppm; -40 to +125°C; 15 mA reference input-current value.	CLKIN support · VDD · load · duty cycle · OE
10-250 MHz + low-jitter CMOS clock	FCO-3P-UJ	3225 6-SMD; CMOS; 2.5 / 3.3 V; ± 25 ppm; -40 to +105°C; 0.8 ps reference phase-jitter value.	Exact frequency · integration band · guaranteed jitter · load
100-220 MHz + differential + ultra-low jitter	FCO-2L-UJ	2520 6-SMD; LVPECL / LVDS / HCSL; 1.8 / 2.5 / 3.3 V; ± 20 ppm; -40 to +125°C; 50 fs reference phase-jitter value.	Output format · SSC · termination · receiver mask · jitter band
32.768 kHz passive or driven timing	FCT-1S FCO-6K-UC	FCT-1S: 1210, CL 6-12.5 pF, ESR 70-90 k Ω . FCO-6K-UC: 2016 CMOS, 1.5 / 1.8 V, 1.4-1.8 μ A, ± 20 ppm.	XTAL loop versus driven input · startup · standby power
Defined 2.4 GHz discrete-filter position	FSF1109-2442M-79M-1.2-40	CSP1109; 2442 MHz center; 79 MHz bandwidth; 1.2 dB insertion loss; 40 dB stopband attenuation.	Impedance · pinout · matching · power · coexistence mask

Selection boundary: phase-jitter figures in this guide are reference values. Guaranteed limits, integration bands, exact ordering codes, lifecycle and interface compliance are confirmed in the applicable FCom specification and quotation.

ENGINEERING SELECTION SUPPORT

Request an FCom PC & Gaming Timing Recommendation

Provide the target processor, hub, PHY, bridge, wireless SoC, controller, PCIe receiver or RF front-end part number together with its clock or filter interface and operating requirements.

[Start Engineering Review →](#)

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Engineering Validation & Minimum RFQ

PC and gaming timing is defined by the receiving device, clock topology, interface compliance and complete electrical environment - not by nominal frequency alone.

Processor / PCIe

- Exact processor, PCH, root-complex or endpoint P/N
- Fixed crystal, platform clock or local XO
- Common-clock / SRNS / SRIS topology
- SSC and PCIe generation
- Output logic, termination and jitter mask

USB / Ethernet / Display

- Hub, PHY or bridge P/N
- XTAL pins or driven CLKIN
- 24 / 25 MHz input or 125 MHz direction
- CL / ESR or VDD / logic / load
- Startup, ppm and temperature limits

Wireless / Controller

- Radio / MCU / module P/N
- HFXO and LFXO requirements
- Frequency, CL, ESR, drive and accuracy
- Sleep / wake and clock switching
- Module-integrated or host-board timing

System / Program

- Board schematic and clock-tree diagram
- Temperature, shock / vibration and EMI
- Prototype quantity and sample date
- Annual volume and lifecycle target
- Compliance and production requirements

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Processor fixed reference, PCIe, USB hub, Ethernet PHY, display bridge, wireless SoC, controller RTC or RF-filter position.
Target Device	Exact receiving IC or module part number, relevant pin name and schematic location.
Clock Topology	Passive crystal, local CMOS XO, differential REFCLK, shared platform clock, internally derived clock or external 32.768 kHz source.
Crystal Requirements	Frequency, package, CL, ESR, C0 where applicable, tolerance / stability, drive level, startup and operating temperature.
XO Requirements	Frequency, VDD, output logic, load, OE, duty cycle, stability, phase jitter / noise, integration band and SSC mode.
RF Filter Requirements	Center frequency, bandwidth, insertion loss, rejection mask, impedance, pinout, matching, input power and coexistence architecture.
Program Requirements	Prototype quantity, requested sample date, validation plan, annual volume, production site, lifecycle and compliance documentation.

Derived Clocks Matter

Confirm whether a platform clock generator or PHY already creates the required 100 or 125 MHz clock.

Jitter Must Be Comparable

A femtosecond headline is meaningful only with aligned output, integration band, voltage, load and test conditions.

Startup Is a Board Result

Crystal start-up margin depends on the oscillator loop, parasitics, layout, drive and production variation.

Frequency alone does not define the final part: the receiving device, topology, output interface, power state and validated jitter or RF mask determine the appropriate FCom configuration.

09

Engineering FAQ & Application Review

Common PC and gaming clock-selection questions, representative public references and the information required for an FCom engineering recommendation.

Is CPU or GPU frequency the external crystal frequency?

No. Multi-gigahertz operating clocks are synthesized internally from one or more lower-frequency references.

Is every 100 MHz oscillator suitable for PCIe?

No. Output format, topology, SSC, phase-jitter mask, common mode, termination and PCIe generation must all be satisfied.

Does USB 5 or 10 Gb/s define the hub crystal?

No. Public USB hub examples use a separate local reference such as 24 MHz, independent of link throughput.

Does Gigabit Ethernet require a 125 MHz XO?

Not necessarily. Many PHYs use a 25 MHz crystal and derive or export 125 MHz internally.

Can one 24 / 25 MHz crystal be copied across devices?

Not automatically. Each oscillator loop has its own CL, ESR, drive, startup and PCB-parasitic requirements.

When is a low-jitter CMOS XO appropriate?

When a peripheral or high-speed receiver exposes a CMOS CLKIN and its complete jitter budget justifies a dedicated source.

When is 32.768 kHz required?

Only where an embedded controller, wireless SoC or RTC exposes an external low-frequency oscillator loop or driven input.

Is a 2.4 GHz SAW filter always required?

No. It is used only where the selected radio architecture provides a discrete filter position matching the required RF mask.

Representative Public Technical References

1. **Intel:** Core Ultra / Meteor Lake clock topology - 38.4 MHz fixed clock and 100 MHz PCIe reference.
2. **Texas Instruments:** TUSB8041EVM - four-port USB 3.0 hub reference platform.
3. **Texas Instruments:** TUSB8041EVM user guide - 24 MHz crystal and external-clock requirements.
4. **Texas Instruments:** DP83867ERGS-R-EVM - 25 MHz crystal and derived 125 MHz reference architecture.
5. **Texas Instruments:** SN65DSI86 - public display-bridge REFCLK options.
6. **Nordic Semiconductor:** nRF5340 oscillator documentation - 32 MHz HF XO and 32.768 kHz LF XO.
7. **Nordic Semiconductor:** nRF7002 DK - public 32.768 kHz crystal implementation.
8. **Intel FPGA:** 10G Ethernet hardware design example - conditional 156.25 MHz reference context.

FCom product specification note: crystal and oscillator information in this guide is presented at series or representative-configuration level unless a complete SAW filter P/N is shown. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom specification and quotation.

ENGINEERING REVIEW

PC, Gaming & Consumer Computing Timing Review

Provide the target processor, hub, PHY, bridge, wireless SoC, controller, PCIe receiver, RTC or RF front-end part number together with its clock or filter interface, frequency, electrical limits, operating temperature, package and project stage.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.