

PRECISION MEASUREMENT TIMING

Oscilloscopes, Digitizers & Data Acquisition

High-speed waveform acquisition and converter-based measurement systems requiring accurate timebase and low-jitter sampling clocks.

Precision Timebase + Low-Jitter Sampling + Trigger Accuracy + Measurement Synchronization



Application Scope

Bench and modular instruments that acquire, digitize, process and synchronize high-speed waveforms across one or multiple measurement channels.

Selection Philosophy

Select by timing layer first. Instrument timebase, converter sampling, FPGA / JESD reference and trigger synchronization can require very different accuracy, phase-noise and jitter performance.

Timebase

Master reference, external reference I/O and long-term measurement accuracy.

Sampling

ADC / DAC clock quality and jitter-limited measurement performance.

Processing

FPGA, JESD, SerDes and digital clock-tree references.

Synchronization

Trigger alignment, common clock distribution and multi-channel skew control.

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Application Scope & Engineering Domains

Separate reference accuracy, sampling jitter, digital clocking and synchronization before assigning a discrete timing component.

Measurement timing is hierarchical. A high-speed digitizer may combine a precision reference (often 10 MHz), a platform- or architecture-defined board reference such as 100 / 125 / 156.25 MHz, and a substantially higher converter sampling clock. The exact frequencies are defined by the selected platform and clock architecture.

Typical Equipment

Oscilloscopes

Digital Oscilloscopes
Mixed-Signal Oscilloscopes
Sampling Oscilloscopes
Protocol / Logic Analysis Hardware

Digitizers

High-Speed Digitizers
PXI / PXIe Digitizers
Modular Acquisition Cards
Multi-Channel Capture Systems

Data Acquisition

Precision DAQ
High-Speed ADC / DAC Systems
Converter Evaluation Platforms
Synchronized Measurement Systems

Five Timing Domains

Precision Timebase

Frequency accuracy · temperature stability · aging · close-in phase noise.

Sampling Clock

RMS jitter · phase noise · differential interface · clock-tree architecture.

FPGA / JESD

REFCLK · SYSREF relationship · SerDes clocking · signal integrity.

Trigger Timing

Trigger uncertainty · timestamping · deterministic acquisition alignment.

Multi-Instrument Synchronization

External reference input / output, common reference distribution, multi-card synchronization and phase-coherent acquisition.

Important Boundary

ADC sample rate, effective sample rate, FPGA processing rate and internal timebase frequency are typically derived from the instrument clock architecture rather than defined directly by a discrete oscillator.

JITTER-LIMITED SNR

$$\text{SNR}_{\text{jitter}} \approx -20 \log_{10}(2\pi \cdot f_{\text{IN}} \cdot t_{\text{J}})$$

For a sinewave in a jitter-limited case, higher analog input frequency produces a greater SNR penalty. Here, t_{J} is the total RMS sampling-time uncertainty—including the relevant external clock, clock-tree and ADC aperture contributions—evaluated over consistent conditions and integration bandwidth.

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Select by System Node First

Identify whether the node is a master timebase, board reference, converter clock, tunable PLL reference or derived timing signal.

System Node	Typical Function	Representative Frequency	Typical Device Type	Selection Focus
Master Timebase	Instrument accuracy / calibration	10 MHz class	OCXO / high-stability TCXO	Accuracy · aging · temperature · phase noise
External Reference I/O	Multi-instrument synchronization	10 MHz	Precision oscillator / reference distribution	Frequency accuracy · output compatibility · phase coherence
PXle Backplane Reference	Modular acquisition clock tree	100 MHz	Chassis clock source / PLL / distribution; local XO where required by the module design	PXle_CLK100 interface · jitter · logic standard · skew
Converter / JESD Reference	Clock-synthesizer input	125 MHz example	Low-jitter XO	Confirm IC architecture · phase noise · PLL multiplication
FPGA / SerDes REFCLK	High-speed digital transfer	156.25 MHz example	Low-jitter differential XO	Confirm protocol / transceiver · logic · jitter · signal integrity
Direct High-Speed Clock	Selected ADC / FPGA clock nodes	250 / 500 MHz	Differential XO / clock synthesizer	Confirm direct clock requirement and system jitter budget
Tunable PLL Reference	Clock discipline / loop control	Architecture dependent	VCXO	Pullability · control range · phase-noise requirement
Direct Sample Clock	Converter sampling	1 GHz class	Clock synthesizer / external source	Confirm the actual external clock requirement independently from the sample rate
Trigger / Timestamp	Acquisition alignment	Derived / distributed	Clock / trigger distribution	Skew · deterministic alignment · jitter

Timebase First

For precision instruments, establish the required accuracy and stability of the master reference before considering downstream clock multiplication.

Sampling Performance

Sampling-clock jitter should be evaluated with the ADC / DAC, analog input frequency, SNR / ENOB target and the specified phase-noise integration bandwidth.

Synchronization

A common frequency reference is only one part of coherent acquisition; trigger distribution, phase alignment and inter-channel skew should also be managed as part of the synchronization architecture.

Recommended selection sequence: System node → external vs derived clock → frequency → accuracy / jitter target → output interface → PLL / pullability requirement → temperature / package → FCom series.

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Frequency & Component Placement Matrix

Keep precision references and board-level oscillator frequencies separate from PLL-generated converter clocks and instrument sample rates.

Frequency Class	System Position	Representative Role	Typical Device	Engineering Focus
COMMON 10 MHz	Master timebase / external reference	Instrument accuracy, calibration and synchronization where specified	OCXO / high-stability TCXO	ppb-level stability where required · aging · close-in phase noise
PLATFORM 100 MHz	PXIe backplane / modular acquisition	PXIe_CLK100 or architecture-defined board reference	Chassis clock source / PLL / distribution	Differential interface · RMS jitter · skew · backplane compliance
EXAMPLE 125 MHz	Converter / JESD clock tree	Possible reference into clock synthesizer / distribution	Low-jitter XO	Confirm converter and clock-IC architecture · PLL multiplication
EXAMPLE 156.25 MHz	FPGA / SerDes REFCLK	Protocol- and transceiver-dependent digital reference	Low-jitter differential XO	LVDS / LVPECL / HCSL · jitter · SI
EXTENSION 250 / 500 MHz	Direct converter / FPGA clock	Architecture-dependent high-speed reference	Differential XO / synthesizer	Direct clock requirement · jitter budget · clock-tree topology
DERIVED 1 GHz / 2.5 GHz+	Sample clock / internal timebase	PLL-generated or internal high-speed timing	Clock synthesizer / internal clock tree	Typically generated within the clock tree rather than used as a default discrete oscillator frequency
DERIVED Sample / Trigger Rates	ADC / DSP / trigger logic	Measurement and processing rates	Generated from upstream clock	Verify the corresponding upstream external reference node

Accuracy Domain

10 MHz precision references are selected primarily for timebase accuracy, stability, aging and phase-noise performance.

Jitter Domain

When the architecture specifies 100 / 125 / 156.25 MHz, board references are selected primarily for jitter, interface compatibility and clock-distribution integrity.

High-Speed Extension

250 / 500 MHz and above require confirmation of the actual direct-clock node. Many instruments synthesize these frequencies from a lower-frequency precision reference.

Comparison note: RMS phase-jitter values are meaningful only when the carrier frequency, supply voltage, output logic and integration bandwidth are defined. Use the applicable FCom datasheet for final jitter-budget validation.

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Representative Platform & Architecture Matrix

Public measurement platforms illustrate how precision references, sampling clocks, converter rates and synchronization are separated in real acquisition systems.

TEKTRONIX

4 Series B MSO · Precision Oscilloscope Timebase

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Architecture: bench oscilloscope with precision timebase, acquisition clocking, trigger processing and internal reference distribution.

Public clock evidence: the timebase can phase-lock to an external **10 MHz** reference; the auxiliary output can provide the oscilloscope reference clock.

10 MHz External Ref → Timebase → Acquisition / Trigger

Engineering insight: instrument timebase frequency and waveform sample rate belong to different timing layers.

NATIONAL INSTRUMENTS

PXIe-5763 · Modular High-Speed Digitizer

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Architecture: PXIe digitizer with onboard reference, reference PLL and selectable internal / external sample-clock operation.

Public clock evidence: supports **10 MHz** reference / PXI_CLK10 and a **1 GHz** external sample clock while the ADC operates at **500 MS/s**.

10 MHz Ref → PLL / Clock Tree → 500 MS/s ADC

Engineering insight: reference frequency, sample-clock frequency and converter sample rate are separate timing parameters and should be specified independently.

ANALOG DEVICES

AD-FMCDQA2-EBZ · JESD204B Converter Clock Tree

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Architecture: precision reference → clock synthesizer → high-speed ADC / DAC clocks, FPGA reference and SYSREF.

Public clock evidence: a **125 MHz** crystal reference feeds the AD9523-1, which generates **1 GHz** ADC / DAC clocks and a **500 MHz** FPGA reference.

125 MHz → AD9523-1 → 1 GHz / 500 MHz

Engineering insight: a lower-frequency precision reference can generate multiple higher-frequency converter and FPGA clocks.

SPECTRUM INSTRUMENTATION

M5i.33xx + Star-Hub · Synchronized Multi-Channel Digitizer

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Architecture: common reference / clock master → synchronized sampling clocks and trigger distribution across multiple acquisition cards.

Public clock evidence: the platform supports an external reference such as **10 MHz**; Star-Hub distributes common clock and trigger with skew management across digitizers.

10 MHz Ref → Master / PLL → Clock + Trigger

Engineering insight: coherent multi-channel acquisition depends on common clock, trigger alignment and skew management.

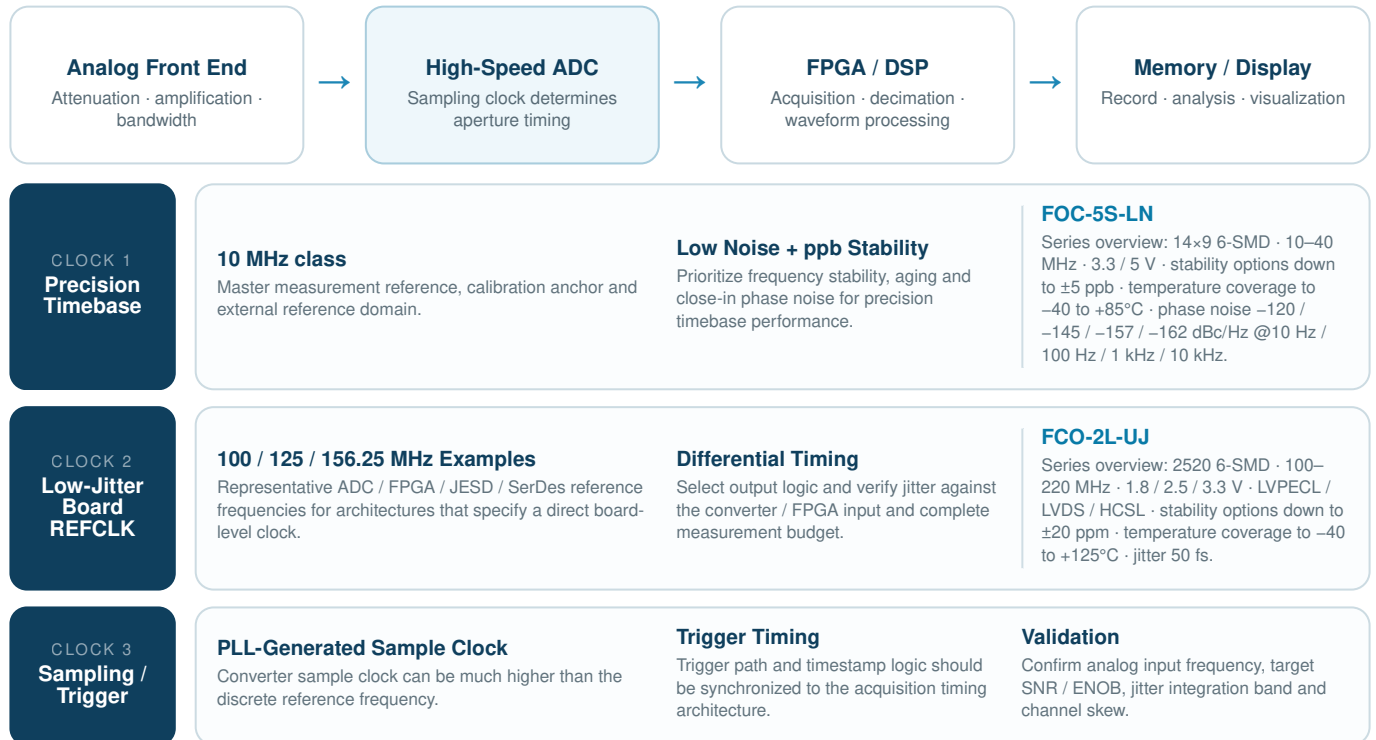
Platform reference note: public third-party platforms are included to illustrate representative timing architectures. Component selection should be completed against the latest target-device documentation, the applicable FCom datasheet and system-level validation requirements.

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Real-Time Digital Oscilloscope Timing Architecture

Representative real-time architecture: the precision timebase establishes the measurement reference while PLL / jitter-cleaning and acquisition domains preserve clock quality. Equivalent-time sampling oscilloscopes use a different strobe / sampling architecture.

Representative Signal & Timing Path



Selection guidance: for designs targeting 50 fs jitter performance, confirm carrier frequency, output format, supply voltage and integration bandwidth against the applicable datasheet and order code. Higher sampling clocks may be synthesized downstream and should be evaluated as part of the complete clock tree.

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Multi-Channel Digitizer & Synchronized DAQ

A coherent acquisition system combines a common precision reference, clock synthesis / distribution, trigger alignment and controlled channel-to-channel skew.

Representative Architecture



Architecture note: 250 / 500 MHz direct clocking is applicable where the target ADC / FPGA clock input requires an externally supplied high-frequency reference and the complete jitter budget supports that implementation.

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FCom Selection Guidance by Design Condition

Representative FCom series are aligned to timing nodes using the FCom Product Selection Matrix. Series-level specifications summarize available options; FCom will confirm the compatible combination and final ordering code for each design.

Precision Timebase
OCXO / high-stability TCXO by stability, phase noise, warm-up and power.

Low-Jitter REFCLK
100–220 MHz differential reference with 50 fs jitter performance.

High-Frequency Extension
Direct differential reference to 1.5 GHz with 0.6 ps jitter performance.

Pullable Reference
VCXO for architectures that explicitly require loop-control pullability.

Design Condition	Representative FCom Series	Series Specification Overview	Selection Relevance
10 MHz precision timebase: stability first	FOC-5S-LN FVT-7S-WT	FOC-5S-LN: 14×9 6-SMD · 10–40 MHz · 3.3 / 5 V · rectangular · stability options down to ±5 ppb · temperature coverage to –40...+85°C · PN –120 / –145 / –157 / –162 dBc/Hz @10 / 100 / 1k / 10k. FVT-7S-WT: 7050 4-SMD · 10–52 MHz · 2.5 / 3.3 V · clipped sine / CMOS · stability options down to ±50 ppb · temperature coverage to –40...+105°C · VCTCXO pullability ±5 ppm.	FOC-5S-LN supports designs prioritizing low noise and high timebase stability; FVT-7S-WT is suited to designs emphasizing compact size, lower power, faster start-up or extended temperature coverage.
100 / 125 / 156.25 MHz differential REFCLK, when specified	FCO-2L-UJ	2520 6-SMD · 100–220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · stability options down to ±20 ppm · temperature coverage to –40...+125°C · 50 fs jitter .	Suitable for ADC / FPGA / JESD / SerDes reference nodes that match the supported frequency, interface and validated jitter conditions.
250 / 500 MHz or higher direct differential clock	FCO-3L-PG	3225 6-SMD · 10–1500 MHz · 2.5 / 3.3 V · LVPECL / LVDS · stability options down to ±25 ppm · temperature coverage to –40...+105°C · 0.6 ps jitter .	Suitable for architecture-defined high-frequency clock nodes where the receiver requires a direct differential clock and the system jitter budget supports the selected configuration.
PLL / clock-discipline loop requires pullability	FVC-3L-PG	3225 6-SMD · 10–1500 MHz · 2.5 / 3.3 V · LVPECL / LVDS · stability options ±25 to ±50 ppm · temperature coverage to –40...+105°C · pullability options ±50 to ±150 ppm.	Designed for PLL and synchronization architectures that require voltage-controlled frequency adjustment.

ORDERING NOTE Series tables summarize the best available stability, widest temperature coverage and representative jitter / phase-noise values across each product family. Availability varies by frequency, supply voltage, output and temperature grade. FCom will confirm the compatible specification combination and final order code for the target design.

ENGINEERING SELECTION SUPPORT

Request an FCom Measurement-Timing Recommendation

Provide the target ADC / DAC / FPGA / clock device, clock node, frequency, output logic, jitter / phase-noise requirement, temperature range and synchronization architecture.

Start Engineering Review →

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Engineering Validation & RFQ Checklist

Translate the measurement-performance target into timebase accuracy, clock-jitter, interface and synchronization requirements before final component and ordering-code selection.

Precision Timebase

- Nominal reference frequency
- Required frequency accuracy / stability
- Operating temperature
- Aging requirement
- Close-in phase-noise requirement
- Output type / level
- Calibration / external-reference architecture

Sampling Clock

- Exact ADC / DAC P/N
- Clock-input frequency
- Maximum analog input frequency
- Target SNR / ENOB
- RMS jitter target and integration bandwidth
- LVDS / LVPECL / HCSL / CMOS
- Direct clock vs PLL-generated clock

FPGA / JESD / SerDes

- FPGA / transceiver P/N
- REFCLK frequency
- JESD204 subclass / SYSREF architecture
- Clock fan-out topology
- Logic voltage and termination
- Allowed frequency tolerance
- Signal-integrity constraints

Synchronization

- Channel / board count
- Common 10 MHz reference?
- Trigger distribution topology
- Channel-to-channel skew target
- Phase coherence requirement
- Timestamp / deterministic-latency requirement
- Cable / backplane distribution

Minimum RFQ Information

Information Category	What to Provide
Instrument / Platform	Oscilloscope, digitizer, PXI / PXIe module, DAQ, converter card or synchronized multi-channel system.
Target Clock Node	Exact IC and XTAL / REFCLK / MCLK / CLKIN / external-reference / sample-clock pin or schematic location.
Frequency	External reference frequency and separately the downstream sample / processing frequency if different.
Performance	Frequency stability, phase noise, RMS jitter integration band, analog input frequency, SNR / ENOB and skew targets.
Electrical Interface	VDD, CMOS / LVDS / LVPECL / HCSL, load / termination, OE / standby and pullability where required.
Environment	Operating temperature, warm-up / calibration constraints, airflow / enclosure conditions and lifecycle requirements.
Program	Prototype quantity, sample date, EAU, production location and qualification / documentation requirements.

Jitter-budget input: for high-speed converter applications, include the maximum analog input frequency—not only the ADC sample rate. This is essential for evaluating clock-jitter contribution to measurement SNR.

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Engineering FAQ & Application Review

Common interpretation questions for oscilloscope, digitizer and data-acquisition timing architectures.

Is ADC sample rate the oscillator frequency?

Not necessarily. Sample rate may equal, divide from or be synthesized from a supplied clock. The discrete timing device should be selected from the documented reference / clock-input requirement.

Why does clock jitter matter more at high input frequency?

For a given RMS jitter level, the jitter-limited SNR decreases as the analog input frequency increases. The clock should therefore be evaluated against the actual measurement bandwidth.

Does lower phase noise at one offset always mean lower RMS jitter?

No. RMS phase jitter depends on the integrated phase-noise spectrum and the specified integration bandwidth. Meaningful comparisons require consistent carrier, output, supply and measurement conditions.

When is an OCXO appropriate?

When the master timebase requires very tight frequency stability, low drift and low phase noise beyond the standard XO / TCXO class supported by the instrument architecture.

When should a differential XO be used?

Where the ADC / FPGA / SerDes clock input specifies LVDS, LVPECL or HCSL, or where the system clock architecture requires a low-jitter differential reference.

Does every ADC need its own oscillator?

Not necessarily. Multiple converters may share a synthesized or distributed clock. The appropriate timing component depends on the complete clock tree and synchronization topology.

Representative Public Technical References

1. **Tektronix:** 4 Series B MSO — precision timebase and external 10 MHz reference architecture.
2. **National Instruments:** PXIe-5763 — reference-clock, external sample-clock and digitizer sampling specifications.
3. **PXI Systems Alliance:** PXI Express Hardware Specification — PXIe_CLK100 backplane clock definition.
4. **Analog Devices:** AD-FMCDQA2 / JESD204B clock-tree architecture — 125 MHz reference, converter clocks, FPGA REFCLK and SYSREF.
5. **Spectrum Instrumentation:** M5i Star-Hub — common clock and trigger distribution for synchronized digitizers.
6. **FCom:** Product Selection Matrix, Rev 2026-08 — category, package, frequency, supply, stability, temperature, output, jitter / phase-noise and mounting information for the selected series.

FCom specification basis: product values in this guide follow the FCom Product Selection Matrix. Series-level values summarize available options across each family. During engineering review, FCom will confirm the applicable datasheet, compatible specification combination, jitter / phase-noise conditions, electrical configuration and final ordering code.

ENGINEERING REVIEW

Oscilloscope, Digitizer & DAQ Timing Review

Share the timebase, converter, FPGA and synchronization architecture together with frequency, accuracy, jitter, phase-noise, temperature and output-interface requirements. FCom can review the timing hierarchy and recommend an appropriate series and configuration.

[Request Engineering Review](#)



[FCom Solutions](#)

Third-party names and publicly documented platforms are referenced solely to illustrate representative timing architectures. They are not intended to indicate affiliation, endorsement, qualification or a confirmed FCom design-in. Final selection should follow the latest target-device documentation, the applicable FCom datasheet and system-level validation.