

OPTICAL MODULES & HIGH-SPEED ETHERNET

Optical Modules & High-Speed Ethernet

Engineering guidance for high-speed optical modules, optical interconnects and data-center Ethernet links across host SerDes, QSFP-DD, OSFP, module DSP, gearbox and retimer clock domains.

Define the Physical Clock Node + Preserve Link Margin + Control Integrated Jitter

100G / 400G / 800G

QSFP28 / QSFP-DD

OSFP

156.25 / 161.1328125 MHz

312.5 / 322.265625 MHz

625 MHz Review

Application Scope

Switch and FPGA host boards, line cards, retimer channels, QSFP28 / QSFP-DD / OSFP modules, optical DSPs, gearboxes, laser-driver interfaces and optical engines.

Selection Approach

Selection begins at the physical clock input that requires an external timing component. Host SerDes references, module-DSP references, management clocks and recovered clocks remain separate functions even when they share the same system.

Host SerDes

156.25 or exact 161.1328125 MHz differential reference.

Module DSP

312.5, 322.265625, 325.50 or conditional 625 MHz.

Board & Control

25 / 50 / 100 / 125 MHz where a driven input is exposed.

CDR Boundary

Some retimers require an external reference, while others operate without one.

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Application Scope & Engineering Domains

A high-speed optical link can contain several independent timing boundaries from the host reference through the pluggable module and optical engine.

One link, multiple clock trees. The host SerDes reference, clock-generator output, recovered retimer timing, module-DSP reference and lower-speed management clock are distinct component positions and are not automatically interchangeable.

Representative System Scope

Host & Line Card

Ethernet switch ASIC
FPGA transceiver bank
Network interface card
Line card / backplane
QSFP-facing SerDes

Pluggable Optical Module

QSFP28 / QSFP-DD
OSFP module
Module DSP / gearbox
Laser driver / SiPho
DR4 / FR4 optical engine

Channel & Support

Retimer / CDR
Clock generator / fan-out
Module controller / CMIS
Management PHY
Power and thermal domain

Four Engineering Domains

Host SerDes Reference

Differential logic, termination, common mode, phase-jitter band and PLL transfer function.

Retimer / CDR Boundary

External-reference requirement is device-specific; recovered timing may eliminate the XO position.

Module DSP Reference

Exact high frequency, jitter mask, startup, current, package height and module thermal budget.

Management Domain

Use a driven CMOS clock or passive crystal circuit only where the controller documentation supports that operating mode.

Host Reference

156.25 /
161.1328125 MHz



Switch / FPGA

MAC · PCS · FEC ·
SerDes



Retimer / Channel

CDR · equalization ·
signal recovery



QSFP / OSFP

Electrical host
interface



Optical Link

DSP · laser · fiber

Exact Frequency

Preserve all digits of
161.1328125 and
322.265625 MHz; do not
substitute nearby values.

Output Interface

Define LVDS, LVPECL,
HCSL or CMOS, supply,
swing, common mode
and coupling.

Jitter Definition

State carrier, integration
band, mask, spurs,
receiver PLL bandwidth
and distribution path.

Module Environment

Confirm package height,
current, startup, supply
noise, airflow and end-
product temperature.

Architecture boundary: Ethernet line rate is not oscillator frequency. Internally generated, source-synchronous and recovered clocks should not be assigned a standalone oscillator unless the device documentation identifies a physical external input.

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Select by System Node First

Identify the physical clock function and receiving interface before comparing oscillator series or nominal frequency coverage.

System Node	Clock Role	Representative Frequency	Typical Device	Selection Focus
Host FPGA / Switch SerDes	Externally driven high-speed reference	156.25 MHz	Low-jitter differential XO or clock-generator output	logic · VCC · termination · common mode · jitter band · PLL transfer
Alternative SerDes Plan	Exact configured transceiver reference	161.1328125 MHz	Exact-frequency differential XO	all frequency digits · divider setting · interface · mask · integration band
PAM4 / Module DSP	Gearbox or optical-DSP synthesis reference	312.5 / 322.265625 MHz	Wide-frequency differential XO	exact input option · high-offset jitter · spurs · package power · thermal limit
Platform-Specific PAM4 / DSP	Selected FPGA bank or 800G module input	325.50 / 625 MHz	Conditional high-frequency differential source	device input specification · VCC · logic · phase-noise mask · startup
Module Controller / Housekeeping	Local MCU, PHY or clock-controller input	25 / 50 / 100 / 125 MHz	CMOS XO or documented passive crystal	source direction · oscillator mode · VDD · load · duty cycle · OE · startup
Data-Recovery Retimer	Independent CDR locked to serial data	No external reference	No external oscillator when the retimer documentation confirms reference-free operation	confirm the exact retimer, then review the adjacent host and module clock boundaries

1 · Confirm the Physical Node

Use the schematic and device clock tree to determine whether an external clock input requiring a discrete timing component is present.

2 · Define the Electrical Budget

Specify exact frequency, supply, output format, termination, receiver bias, coupling, load and enable behavior.

3 · Validate the Link

Measure phase noise, integrated jitter, BER, FEC margin, restart and thermal performance on the final platform.

Recommended sequence: System node → physical input → source direction → exact frequency → output interface → jitter / phase-noise budget → environment → FCom configuration and ordering-code confirmation.

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Frequency & Component Placement Matrix

Frequency becomes meaningful only when it is tied to the physical clock position, receiver mode and source direction.

Frequency	Representative Position	Public Architecture Context	Required Function	Key Engineering Check
25 / 50 MHz Conditional	Module MCU, management PHY or clock-controller reference	Housekeeping and control domain; not the high-speed lane reference	CMOS XO or passive crystal only where the input mode is documented	direction · VDD · logic · CL / ESR if passive · duty cycle · startup
100 / 125 MHz Board Ref	Host board, FPGA system clock or selected supporting Ethernet domain	Legacy or supporting programmable clock trees	CMOS or differential XO according to the receiver	do not merge SYSCLK, PCIe or SerDes positions solely because the nominal frequencies match
156.25 MHz Primary	High-speed Ethernet SerDes and QSFP-facing transceiver bank	AMD VH158 and Intel Agilex 7 F-Tile NRZ clocking	Low-jitter differential XO or multi-output generator path	LVDS / LVPECL / HCSL · termination · jitter band · mask · PLL transfer
161.1328125 MHz SerDes Ref	Alternative Ethernet SerDes reference plan	Selected 10.3125 / 25.78125 Gb/s FPGA configurations	Exact-frequency low-jitter differential XO	preserve all digits · confirm divider · interface · receiver mask
312.5 / 322.265625 MHz PAM4 / DSP	High-rate SerDes, gearbox or optical-module DSP	Published FPGA options and module-DSP synthesis architectures	Wide-frequency differential XO with jitter verified against the target device	input level · VCC · integration band · phase-noise mask · thermal limits
325.50 / 625 MHz Platform-Specific	56 Gb/s PAM4 FPGA bank or selected 800G module DSP	Intel Agilex 7 I-Series and Broadcom BCM83822	Conditional high-frequency differential reference	do not substitute nearby frequencies · confirm interface and power budget
Recovered Clock No XO	Retimer CDR and internal clock recovery	TI DS280DF810 locks each data channel without a low-jitter reference	No external oscillator when the documented architecture does not require one	verify the exact device; the no-reference conclusion is device-specific

156.25 MHz

Main public host-SerDes reference opportunity.

161.1328125

Exact alternative SerDes plan; never round the value.

312.5-625

Higher-frequency DSP review requires device-level data.

Recovered Clock

No external oscillator when the CDR requires no external source.

Placement rule: nominal frequency coverage does not establish compatibility. The exact receiving device, physical input, output interface, jitter definition, supply environment and clock-distribution path determine the appropriate product class and configuration.

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Representative Platform & Architecture Matrix

Four public platforms illustrate a host SerDes reference, dual-QSFP-DD clock tree, module-DSP reference and retimer that operates without an external low-jitter reference clock.

AMD

Versal HBM VHK158 Evaluation Kit 1

Architecture: VH1582 adaptive SoC, 112G PAM4 transceivers, QSFP28 and QSFP-DD connectivity.

Public clock evidence: U299 RC21008A provides default 156.25 MHz, 1.8 V LVDS references to the high-speed transceiver banks.

156.25 MHz LVDS → Versal GTY / GTM → QSFP28 / QSFP-DD

Selection insight: a fixed low-jitter XO may be evaluated when the production clock tree does not require the board generator's fan-out or programmability.

INTEL / ALTERA

Agilex 7 FPGA I-Series Development Kit 2

Architecture: dual QSFP-DD connectors route to 16 F-Tile FGT channels through a dedicated clock tree.

Public clock evidence: 156.25 MHz is assigned to 28 Gb/s NRZ and exact 325.50 MHz to 56 Gb/s PAM4; Si5391 supplies the QSFP-DD references.

156.25 / 325.50 MHz → Agilex 7 F-Tile → Dual QSFP-DD

Selection insight: preserve 325.50 MHz exactly. The separate 50 MHz MAX 10 controller clock is not an Ethernet SerDes reference.

BROADCOM

BCM83822 800G Optical-Module DSP 3

Architecture: 800G 8:4 PAM4 gearbox / DSP with integrated laser driver for OSFP DR4 and FR4 modules.

Public clock evidence: the device converts eight 106.25 Gb/s client lanes to four 212.5 or 226.875 Gb/s optical-side lanes and publishes 312.5 / 625 MHz clock synthesis.

312.5 / 625 MHz → DSP / FEC / Gearbox → Laser / DR4 / FR4

Selection insight: input logic, VCC, phase-jitter limits, package power and module thermal budget should be confirmed before an FCom series is proposed.

TEXAS INSTRUMENTS

DS280DF810EVM Multi-Rate Retimer 4

Architecture: eight-channel 20.2–28.4 Gb/s retimer with CTLE, DFE, CDR and TX FIR signal conditioning.

Public clock evidence: TI explicitly states that no low-jitter reference clock is required; USB2ANY supports configuration rather than the data-path reference.

Lossy Channel → CTLE / DFE / CDR → Retimed Output

Selection insight: the cited architecture does not require an oscillator at this retimer node. The timing review therefore shifts to the adjacent host SerDes or module-DSP input.

Platform interpretation: third-party platforms are cited solely to illustrate public architectures and physical clock positions. Their inclusion does not imply that a platform vendor has adopted, endorsed, qualified or approved any FCom product, nor does it establish drop-in compatibility.

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Host / FPGA-to-Optical-Module Clock Architecture

Representative path from the host differential reference through switch or FPGA SerDes, channel conditioning and a pluggable optical module.



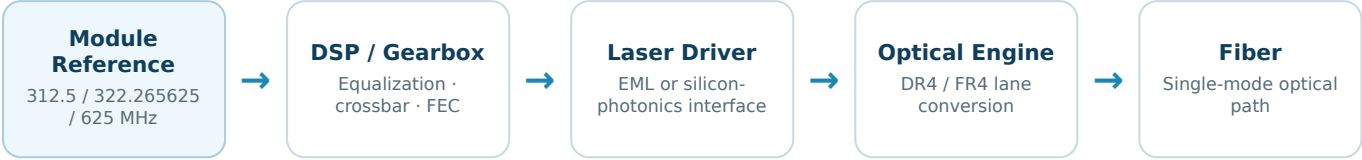
LAYER 1 Host REFCLK	156.25 / 161.1328125 MHz Differential reference to a switch ASIC, FPGA GT bank or QSFP-facing SerDes.	Receiver definition LVDS / LVPECL / HCSL, VCC, common mode, termination, coupling and mask.	Representative FCom option FCO-2L-UJ may be considered, subject to device-level interface and jitter review.
LAYER 2 Distribution	Generator / fan-out / mux Evaluation platforms may distribute several references or support switching and synchronization.	Fixed-source condition A fixed XO may be considered only when fan-out, programmability and redundancy are not required.	Representative FCom options FCO-2L-UJ or FCO-2L may be considered according to the receiver budget.
LAYER 3 Retimer / CDR	Device-specific boundary Some retimers expose an external reference; others recover each channel independently.	Reference-free example TI documentation states that the DS280DF810 requires no low-jitter reference clock.	FCom guidance Do not specify an external oscillator at this node when the exact retimer documentation confirms that no external source is required.
LAYER 4 Management	25 / 50 / 100 / 125 MHz Possible MCU, local PHY or clock-controller input separate from the high-speed lane reference.	Driven-input checks Direction, VDD, VIH / VIL, load, duty cycle, startup and OE behavior.	Representative FCom option FCO-2C may be considered only where the device documentation exposes a compatible CMOS input.
Jitter Transfer Include clock-generator and fan-out additive jitter plus the receiving PLL transfer function.			
Power Integrity Evaluate supply noise, spurs, local decoupling and coupling at the receiver.			
Link Validation Confirm BER, FEC counters, eye margin and restart behavior across traffic and temperature.			

Design rule: a 156.25 MHz frequency match alone does not establish compatibility. The final source must satisfy the target receiver interface and its complete phase-jitter definition.

06

Pluggable-Module DSP & Optical-Engine Architecture

Representative path from a high-frequency module reference through PAM4 DSP / gearbox, laser interface and optical lane conversion.



312.5 / 322.265625 MHz

High-rate PAM4 SerDes, gearbox or optical-DSP reference. Preserve the exact configured value and obtain the device input specification.

Review focus: VCC, input logic, phase-jitter band, phase-noise mask, spurs and startup.

325.50 / 625 MHz

Platform-specific FPGA or 800G module-DSP position. Nominal oscillator range does not establish compatibility.

Review focus: exact frequency, high-offset jitter, package power, height and module thermal budget.

Management / Housekeeping

25 / 50 / 100 / 125 MHz may serve an MCU, PHY or controller input that is electrically separate from the module-DSP reference.

Review focus: driven CMOS mode, supply, load, duty cycle, startup and OE.

CLOCK A DSP Input	312.5-625 MHz family Frequency is selected by the exact DSP / gearbox clock-synthesis architecture.	Thermal integration Current, package height and supply noise are part of the pluggable-module budget.	Representative FCom option FCO-3L-PG may be considered, subject to frequency-specific application engineering review.
CLOCK B Control	25 / 50 / 100 / 125 MHz Possible controller clock where the module schematic exposes a driven input.	Not a SerDes substitute The lower-frequency control clock does not replace the differential DSP reference.	Representative FCom option FCO-2C may be considered after electrical-interface confirmation.
BOUNDARY Recovered	CDR / internal PLL Recovered and internally generated clocks remain system timing functions.	No exposed input No standalone oscillator is assigned when the device provides no physical reference pin.	FCom guidance Continue the timing review at the adjacent host and module clock boundaries.

Architecture note: FCom recommends qualifying the final module source against the DSP receiver, complete clock-distribution path, phase-jitter definition, power-integrity environment and the module’s thermal operating envelope.

07 FCom Selection Guidance by Design Condition

The following FCom series may be considered for four externally implemented clock functions where frequency, interface or jitter performance materially changes the selection.

Ultra-Low-Jitter REFCLK
Host FPGA, switch SerDes and QSPF-facing differential inputs.

Standard Differential Clock
Board references whose receiver jitter budget does not require ultra-low-jitter performance.

High-Frequency DSP Clock
312.5-625 MHz device-specific PAM4 or optical-DSP review.

Driven CMOS Control Clock
Module controller or housekeeping input separate from the data path.

Design Condition	Representative FCom Option	Representative Series Capability	Key Check Before RFQ
100 / 125 / 156.25 / 161.1328125 MHz differential host reference	FCO-2L-UJ	2520 6-SMD · 100-220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · ±20 ppm · -40 to +125°C · 25-65 mA. Representative published family jitter: 50 fs under specified test conditions; confirm carrier, integration band, load and method.	exact frequency · output format · termination · mask · integration band · PLL transfer
General-purpose differential board clock through 220 MHz	FCO-2L	2520 6-SMD · 13.5-220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · ±25 ppm · -40 to +125°C · 20-55 mA. Representative published family jitter: 0.15 ps; confirm test conditions and validate against the target receiver mask.	receiver budget · carrier · integration band · interface · topology · startup
312.5 / 322.265625 / 325.50 / 625 MHz DSP or PAM4 reference	FCO-3L-PG	3225 6-SMD · 10-1500 MHz · 2.5 / 3.3 V · LVPECL / LVDS · 35-50 mA · ±25 ppm · -40 to +105°C. Representative published family jitter: 0.6 ps; the target device and application require separate qualification.	device input · VCC · output logic · high-offset jitter · thermal · package
25 / 50 / 100 / 125 MHz module management clock	FCO-2C	2520 4-SMD · 1.25-125 MHz · 1.8 / 2.5 / 3.3 V · CMOS · ±20 ppm · -40 to +125°C · 1.2-15 mA.	driven input · VDD · levels · load · duty cycle · startup · OE
Retimer with documented no-reference operation	External oscillator not required at retimer	Continue host and module reference selection at the adjacent physical clock boundaries.	exact retimer P/N · manufacturer clock statement · channel architecture

Application boundary: VCXO, TCXO, OCXO, crystal-filter and SAW product families may be considered for project-specific functions but are not standard elements of the four recurring clock positions above. Series identifiers are not complete ordering codes.

ENGINEERING SELECTION SUPPORT

Request an FCom Optical-Clock Recommendation

Provide the host or module clock tree, target switch / FPGA / SerDes / retimer / DSP, exact physical frequency, interface, jitter or phase-noise definition, temperature and project stage.

[Start Engineering Review →](#)

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Engineering Validation & Minimum RFQ

Submit one requirement set for each externally implemented clock position and keep host, module-DSP, management and recovered-clock domains separate.

Platform & Functional Node

- Exact switch ASIC, FPGA, SerDes, retimer, gearbox or optical-DSP P/N
- Host board, line card, QSFP28, QSFP-DD, OSFP or optical-engine boundary
- Physical clock pin, source direction and current reference BOM
- Schematic, clock tree and board / module revision

Electrical Interface

- LVDS, LVPECL, HCSL, CMOS or accepted input format
- Supply, amplitude, common mode, receiver bias and termination
- AC / DC coupling, load, trace impedance and allowed edge rate
- Output enable, standby state and power sequencing

Jitter, Phase Noise & Stability

- RMS and peak limits with explicit integration band
- Phase-noise mask, carrier, offset frequencies and spurs
- Downstream PLL bandwidth and distribution additive jitter
- Initial tolerance, temperature stability, aging and startup

Environment, Program & Qualification

- Operating / storage temperature, airflow, package height and current
- Ethernet rate, modulation, FEC mode and optical reach
- Samples, prototype date, annual volume and program lifetime
- Reliability qualification, reports and change-control scope

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Host SerDes reference, clock-generator source, retimer input, module-DSP reference or separate management clock.
Target Device	Exact receiving IC / module P/N, physical clock pin, schematic location, block diagram and current reference BOM.
Exact Frequency & Topology	All digits of the input frequency; direct XO, generator, fan-out, mux, jitter cleaner or recovered path; number of destinations.
Electrical Requirements	VDD, output logic, swing, common mode, coupling, termination, receiver bias, load, OE and startup behavior.
Timing Requirements	Jitter limit and integration band, phase-noise mask, spurs, PLL bandwidth, stability, aging and total ppm budget.
Environment & Program	Temperature, supply-noise environment, package / height, current, samples, annual volume, qualification and lifecycle.

Electrical Validation

Confirm swing, common mode, termination, coupling, duty cycle, startup and receiver compatibility.

Timing Validation

Measure phase noise, integrated jitter, spurs and supply sensitivity using the defined load and band.

Link Validation

Verify BER, FEC counters, eye margin, restart and thermal performance across production variation.

Frequency alone does not define the final part: the receiving device, source direction, electrical interface, jitter definition, topology and environmental profile determine the appropriate series and configuration.

09

Engineering FAQ & Application Review

Common optical-clock questions, representative public references and the information required for FCom application engineering review.

Is 100G, 400G or 800G the oscillator frequency?

No. These are aggregate Ethernet rates. The physical reference is defined by the selected SerDes or module DSP.

Are 156.25 and 161.1328125 MHz interchangeable?

No. They belong to different reference plans. Preserve all digits and confirm the configured divider.

Can 322.265625 MHz replace 325.50 MHz?

No. The Intel public platform specifies exact 325.50 MHz for its 56 Gb/s PAM4 bank.

Does range coverage qualify FCO-3L-PG for 800G?

No. Frequency range alone does not establish suitability. Input logic, VCC, jitter band, phase-noise mask, startup and module thermal limits must also be reviewed.

Does every retimer need an external oscillator?

No. TI states that DS280DF810 requires no low-jitter reference. Other devices may differ.

When is FCO-2L-UJ preferred over FCO-2L?

FCO-2L-UJ may be considered when the receiver requires the lower published family jitter value, with both series compared under equivalent test conditions.

When are VCXO, TCXO, OCXO or filters considered?

These families should be evaluated only when the selected architecture exposes a defined tuning, holdover or RF / IF filtering function.

Are the listed series complete orderable P/Ns?

No. FCom confirms the complete ordering code based on frequency, supply, output, stability, temperature and qualification requirements.

Representative Public Technical References

1. **AMD:** VHK158 official page and UG1611 clock generation.
2. **Intel / Altera:** network interfaces and clock circuits.
3. **Broadcom:** BCM83822 800G optical-module DSP official page.
4. **Texas Instruments:** DS280DF810 and DS280DF810EVM official pages.
5. **FCom:** Frequency-Control & Timing Solutions portfolio and application-engineering support.

FCom product specification note: information in this guide is presented at series or representative-configuration level. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable product specification and quotation.

ENGINEERING REVIEW

Optical Modules & High-Speed Ethernet Review

Provide the platform, physical clock node, exact frequency, interface, topology, jitter or phase-noise definition, operating temperature and project stage. FCom Application Engineering will review the requirements and propose a suitable series and configuration for system-level validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. FCom confirms the proposed configuration against the latest target-device documentation and applicable FCom product specification; the complete board or optical module must then be validated under the intended operating conditions.