OPTICAL MODULES & HIGH-SPEED ETHERNET

Optical Modules & High-Speed Ethernet

FCom timing solutions for optical modules and high-speed Ethernet, from host SerDes and retimers to module DSPs and optical engines. Includes 312.5 MHz high-fundamental quartz references for 800G designs.

Low Phase Noise · Defined Clock Interfaces · Module-Level Validation

100G / 400G / 800G | QSFP28 / QSFP-DD | OSFP | 156.25 / 161.1328125 MHz | 312.5 / 322.265625 MHz | FCO-6LH / FCO-2LH

Application Scope

Switch and FPGA host boards, line cards, retimer channels, QSFP28 / QSFP-DD / OSFP modules, optical DSPs, gearboxes, laser-driver interfaces and optical engines.

FCom Engineering Approach

Selection begins at the physical clock input that requires an external timing component. Host SerDes references, module-DSP references, management clocks and recovered clocks remain separate functions even when they share the same system.

Host SerDes

156.25 or exact 161.1328125 MHz differential reference.

Module DSP

312.5 MHz: FCO-6LH / FCO-2LH. Other frequencies require a separate configuration.

Board & Control

25 / 50 / 100 / 125 MHz where a driven input is exposed.

CDR Boundary

Some retimers require an external reference, while others operate without one.

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01

Application Scope & Engineering Domains

A high-speed optical link can contain several independent timing boundaries from the host reference through the pluggable module and optical engine.

One link, multiple clock trees. The host SerDes reference, clock-generator output, recovered retimer timing, module-DSP reference and lower-speed management clock are distinct component positions and are not automatically interchangeable.

Representative System Scope

Host & Line Card

Ethernet switch ASIC
FPGA transceiver bank
Network interface card
Line card / backplane
QSFP-facing SerDes

Pluggable Optical Module

QSFP28 / QSFP-DD
OSFP module
Module DSP / gearbox
Laser driver / SiPho
DR4 / FR4 optical engine

Channel & Support

Retimer / CDR
Clock generator / fan-out
Module controller / CMIS
Management PHY
Power and thermal domain

Four Engineering Domains

Host SerDes Reference

Differential logic, termination, common mode, phase-jitter band and PLL transfer function.

Retimer / CDR Boundary

External-reference requirement is device-specific; recovered timing may eliminate the XO position.

Module DSP Reference

Exact high frequency, jitter mask, startup, current, package height and module thermal budget.

Management Domain

Use a driven CMOS clock or passive crystal circuit only where the controller documentation supports that operating mode.

Host Reference
156.25 / 161.1328125 MHz
→
Switch / FPGA
MAC · PCS · FEC · SerDes
→
Retimer / Channel
CDR · equalization · signal recovery
→
QSFP / OSFP
Electrical host interface
→
Optical Link
DSP · laser · fiber

Exact Frequency

Preserve all digits of 161.1328125 and 322.265625 MHz; do not substitute nearby values.

Output Interface

Define LVDS, LVPECL, HCSL or CMOS, supply, swing, common mode and coupling.

Jitter Definition

State carrier, integration band, mask, spurs, receiver PLL bandwidth and distribution path.

Module Environment

Confirm package height, current, startup, supply noise, airflow and end-product temperature.

Architecture boundary: Ethernet line rate is not oscillator frequency. Internally generated, source-synchronous and recovered clocks should not be assigned a standalone oscillator unless the device documentation identifies a physical external input.

02

Select by System Node First

Identify the physical clock function and receiving interface before comparing oscillator series or nominal frequency coverage.

System Node	Clock Role	Representative Frequency	Typical Device	Selection Focus
Host FPGA / Switch SerDes	Externally driven high-speed reference	**156.25 MHz**	Low-jitter differential XO or clock-generator output	logic · VCC · termination · common mode · jitter band · PLL transfer
Alternative SerDes Plan	Exact configured transceiver reference	**161.1328125 MHz**	Exact-frequency differential XO	all frequency digits · divider setting · interface · mask · integration band
PAM4 / Module DSP	Gearbox or optical-DSP synthesis reference	312.5 MHz; 322.265625 MHz by separate selection	FCO-6LH / FCO-2LH at 312.5 MHz	exact input option · high-offset jitter · spurs · package power · thermal limit
Platform-Specific PAM4 / DSP	Selected FPGA bank or 800G module input	**325.50 / 625 MHz**	Conditional high-frequency differential source	device input specification · VCC · logic · phase-noise mask · startup
Module Controller / Housekeeping	Local MCU, PHY or clock-controller input	**25 / 50 / 100 / 125 MHz**	CMOS XO or documented passive crystal	source direction · oscillator mode · VDD · load · duty cycle · OE · startup
Data-Recovery Retimer	Independent CDR locked to serial data	**No external reference**	No external oscillator when the retimer documentation confirms reference-free operation	confirm the exact retimer, then review the adjacent host and module clock boundaries

1 · Confirm the Physical Node

Use the schematic and device clock tree to determine whether an external clock input requiring a discrete timing component is present.

2 · Define the Electrical Budget

Specify exact frequency, supply, output format, termination, receiver bias, coupling, load and enable behavior.

3 · Validate the Link

Measure phase noise, integrated jitter, BER, FEC margin, restart and thermal performance on the final platform.

Recommended sequence: System node → physical input → source direction → exact frequency → output interface → jitter / phase-noise budget → environment → FCom configuration and ordering-code confirmation.

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03

Frequency & Component Placement Matrix

Frequency becomes meaningful only when it is tied to the physical clock position, receiver mode and source direction.

Frequency	Representative Position	Public Architecture Context	Required Function	Key Engineering Check
25 / 50 MHz Conditional	**Module MCU, management PHY or clock-controller reference**	Housekeeping and control domain; not the high-speed lane reference	CMOS XO or passive crystal only where the input mode is documented	direction · VDD · logic · CL / ESR if passive · duty cycle · startup
100 / 125 MHz Board Ref	**Host board, FPGA system clock or selected supporting Ethernet domain**	Legacy or supporting programmable clock trees	CMOS or differential XO according to the receiver	do not merge SYSCLK, PCIe or SerDes positions solely because the nominal frequencies match
156.25 MHz Primary	**High-speed Ethernet SerDes and QSFP-facing transceiver bank**	AMD VHK158 and Intel Agilex 7 F-Tile NRZ clocking	Low-jitter differential XO or multi-output generator path	LVDS / LVPECL / HCSL · termination · jitter band · mask · PLL transfer
161.1328125 MHz SerDes Ref	**Alternative Ethernet SerDes reference plan**	Selected 10.3125 / 25.78125 Gb/s FPGA configurations	Exact-frequency low-jitter differential XO	preserve all digits · confirm divider · interface · receiver mask
312.5 / 322.265625 MHz PAM4 / DSP	**High-rate SerDes, gearbox or optical-module DSP**	Published FPGA options and module-DSP synthesis architectures	Wide-frequency differential XO with jitter verified against the target device	input level · VCC · integration band · phase-noise mask · thermal limits
325.50 / 625 MHz Platform-Specific	**56 Gb/s PAM4 FPGA bank or selected 800G module DSP**	Intel Agilex 7 I-Series and Broadcom BCM83822	Conditional high-frequency differential reference	do not substitute nearby frequencies · confirm interface and power budget
Recovered Clock No XO	**Retimer CDR and internal clock recovery**	TI DS280DF810 locks each data channel without a low-jitter reference	No external oscillator when the documented architecture does not require one	verify the exact device; the no-reference conclusion is device-specific

156.25 MHz

A common host-SerDes reference; select by the receiving input.

161.1328125

Exact alternative SerDes plan; never round the value.

312.5–625

312.5 MHz: FCO-6LH / FCO-2LH. Review other frequencies separately.

Recovered Clock

No external oscillator when the CDR requires no external source.

Placement rule: nominal frequency coverage does not establish compatibility. The exact receiving device, physical input, output interface, jitter definition, supply environment and clock-distribution path determine the appropriate product class and configuration.

04 Representative Platform & Architecture Matrix

Representative host, module and retimer architectures define the clock position. The 312.5 MHz FCom configuration is detailed on page 07.

AMD

Versal HBM VHK158 Evaluation Kit

1

Architecture: VH1582 adaptive SoC, 112G PAM4 transceivers, QSFP28 and QSFP-DD connectivity.

Public clock evidence: U299 RC21008A provides default 156.25 MHz, 1.8 V LVDS references to the high-speed transceiver banks.

156.25 MHz LVDS → Versal GTY / GTM → QSFP28 / QSFP-DD

Selection insight: a fixed low-jitter XO may be evaluated when the production clock tree does not require the board generator's fan-out or programmability.

INTEL / ALTERA

Agilex 7 FPGA I-Series Development Kit

2

Architecture: dual QSFP-DD connectors route to 16 F-Tile FGT channels through a dedicated clock tree.

Public clock evidence: 156.25 MHz is assigned to 28 Gb/s NRZ and exact 325.50 MHz to 56 Gb/s PAM4; Si5391 supplies the QSFP-DD references.

156.25 / 325.50 MHz → Agilex 7 F-Tile → Dual QSFP-DD

Selection insight: preserve 325.50 MHz exactly. The separate 50 MHz MAX 10 controller clock is not an Ethernet SerDes reference.

BROADCOM

BCM83822 800G Optical-Module DSP

3

Architecture: 800G 8:4 PAM4 gearbox / DSP with integrated laser driver for OSFP DR4 and FR4 modules.

Public clock evidence: the device converts eight 106.25 Gb/s client lanes to four 212.5 or 226.875 Gb/s optical-side lanes and publishes 312.5 / 625 MHz clock synthesis.

312.5 / 625 MHz → DSP / FEC / Gearbox → Laser / DR4 / FR4

Selection insight: FCO-6LH and FCO-2LH are 312.5 MHz options for interface and module validation. The 625 MHz input option requires a separate frequency product.

TEXAS INSTRUMENTS

DS280DF810EVM Multi-Rate Retimer

4

Architecture: eight-channel 20.2–28.4 Gb/s retimer with CTLE, DFE, CDR and TX FIR signal conditioning.

Public clock evidence: TI explicitly states that no low-jitter reference clock is required; USB2ANY supports configuration rather than the data-path reference.

Lossy Channel → CTLE / DFE / CDR → Retimed Output

Selection insight: the cited architecture does not require an oscillator at this retimer node. The timing review therefore shifts to the adjacent host SerDes or module-DSP input.

Platform interpretation: third-party platforms are cited solely to illustrate public architectures and physical clock positions. Their inclusion does not imply that a platform vendor has adopted, endorsed, qualified or approved any FCom product, nor does it establish drop-in compatibility.

05

Host / FPGA-to-Optical-Module Clock Architecture

Representative path from the host differential reference through switch or FPGA SerDes, channel conditioning and a pluggable optical module.

LAYER 1 **Host REFCLK**	**156.25 / 161.1328125 MHz** Differential reference to a switch ASIC, FPGA GT bank or QSFP-facing SerDes.	**Receiver definition** LVDS / LVPECL / HCSL, VCC, common mode, termination, coupling and mask.	**Representative FCom option** FCO-2L-UJ is an option for exact-frequency, interface and jitter review. See the UJ family links below.
LAYER 2 **Distribution**	**Generator / fan-out / mux** Evaluation platforms may distribute several references or support switching and synchronization.	**Fixed-source condition** A fixed XO may be considered only when fan-out, programmability and redundancy are not required.	**Representative FCom options** FCO-2L-UJ or the differential-output portfolio may be evaluated against the receiver budget.
LAYER 3 **Retimer / CDR**	**Device-specific boundary** Some retimers expose an external reference; others recover each channel independently.	**Reference-free example** TI documentation states that the DS280DF810 requires no low-jitter reference clock.	**FCom guidance** Do not specify an external oscillator at this node when the exact retimer documentation confirms that no external source is required.
LAYER 4 **Management**	**25 / 50 / 100 / 125 MHz** Possible MCU, local PHY or clock-controller input separate from the high-speed lane reference.	**Driven-input checks** Direction, VDD, VIH / VIL, load, duty cycle, startup and OE behavior.	**Representative FCom option** FCO-2C may be considered only where the device documentation exposes a compatible CMOS input.

Jitter Transfer

Include clock-generator and fan-out additive jitter plus the receiving PLL transfer function.

Power Integrity

Evaluate supply noise, spurs, local decoupling and coupling at the receiver.

Link Validation

Confirm BER, FEC counters, eye margin and restart behavior across traffic and temperature.

Design rule: a 156.25 MHz frequency match alone does not establish compatibility. The final source must satisfy the target receiver interface and its complete phase-jitter definition.

Related host-reference products: FCO-6L-UJ · FCO-2L-UJ · FCO-3L-UJ. Select the exact output, frequency and test conditions from the applicable model specification.

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06

800G Module DSP: 312.5 MHz FCom References

FCO-6LH / FCO-2LH · high-fundamental quartz · compact differential reference clocks

For 800G optical-module designs using a 312.5 MHz local reference, FCom offers FCO-6LH and FCO-2LH high-fundamental differential crystal oscillators. Choose the package and output interface against the DSP REFCLK requirements and module layout.

FCom reference
FCO-6LH / FCO-2LH
312.5 MHz
→
Module DSP
PLL · PAM4 · gearbox · FEC
→
Laser interface
EML / silicon photonics
→
Optical lanes
800G DR4 / FR4 architecture

FCO-6LH · 2016 class

High-fundamental differential XO
2.05 ±0.10 × 1.65 ±0.10 × 0.70 ±0.10 mm
Maximum height: 0.80 mm
312.5 MHz · LVDS / LVPECL

View FCO-6LH product →

FCO-2LH · 2520 class

High-fundamental differential XO
2.50 ±0.10 × 2.00 ±0.10 × 0.92 ±0.10 mm
Maximum height: 1.02 mm
312.5 MHz · LVDS / LVPECL

View FCO-2LH product →

312.5 MHz
Local DSP reference

40 fs Max.
RMS jitter; 12 kHz–20 MHz[1]

±20 ppm
Frequency stability

−40 to +105°C
Operating temperature

[1] LVDS jitter is specified with a 3.3 V test-condition note. Confirm the applicable conditions for 1.8 V and 2.5 V versions. Electrical limits and termination are on page 08.

312.5 MHz in representative 800G DSP designs

DSP / module configuration	Reference selection	FCom application
BCM83822-DIE 8:4; 800G DR4 / FR4	312.5 / 625 MHz supported	Evaluate FCO-6LH or FCO-2LH for the 312.5 MHz mode.
BCM85826-DIE 4:4; 800G DR4	312.5 / 625 MHz supported	Match the DSP input, PLL conditions and selected lane-rate mode.
BCM85812 8:8; 800G optical DSP	156.25 MHz reference	Use a separately selected 156.25 MHz source.

Device count per module

A single DSP with one local reference domain normally uses **one XO per module**. Independent domains require separate sources. A shared XO must include fan-out additive jitter, output loading and enable behavior in the budget.

Frequency and package selection

312.5 MHz follows the DSP synthesis plan. OSFP or QSFP-DD form factor alone does not set the frequency. FCO-6LH / FCO-2LH standard frequencies are 285 and 312.5 MHz; other frequencies require a separate product selection.

Design-in scope: FCom supports source selection and interface review. Final suitability is established on the target PCB and module; platform examples identify clock requirements and do not imply vendor qualification.

07

FCom Electrical Specifications & Board Design

312.5 MHz · LVDS / LVPECL · termination, control and power-integrity requirements

Both LH series share the following electrical configuration and six-terminal functions. Supply, output format, coupling and control timing must match the selected DSP input. Use the actual mechanical outline when defining pads and module clearance.

Parameter	LVDS	LVPECL
Frequency stability / temperature	±20 ppm / −40 to +105°C	±20 ppm / −40 to +105°C
Nominal supply voltage	1.8 / 2.5 / 3.3 V	2.5 / 3.3 V
Operating current	40 mA Max.	65 mA Max.
Output high level VOH	1.6 V Max.	VDD−1.1 V to VDD−0.7 V
Output low level VOL	0.9 V Min.	VDD−1.9 V to VDD−1.5 V
Rise / fall time; 20%–80%	0.4 ns Max.	0.4 ns Max.
RMS phase jitter; 12 kHz–20 MHz	40 fs Max.[1]	40 fs Max.
Duty cycle	45%–55%	45%–55%
Control input thresholds	VIH ≥0.8 × VDD; VIL ≤0.2 × VDD	VIH ≥0.8 × VDD; VIL ≤0.2 × VDD
Standby current	60 µA Max.[2]	60 µA Max.[2]
Output load	100 Ω between OUT and OUTN	50 Ω per output to VDD−2 V
Startup time	10 ms Max.	10 ms Max.
Aging; first year at 25°C	±3 ppm/year	±3 ppm/year

[1] The LVDS jitter test-condition note is 3.3 V; confirm conditions for lower-voltage configurations. [2] Standby current applies to the specified control state. Startup time is distinct from enable-recovery time. General datasheet test environment: 25 ±5°C, 40%–70% RH.

Six-terminal connection: FCO-6LH and FCO-2LH

Pin	1	2	3	4	5	6
Function	E/D	NC	GND	OUT	OUTN	VDD

Keep Pin 2 unconnected. Pins 4 and 5 form the differential pair. Drive Pin 1 to a defined logic level and check the package view and Pin 1 orientation against the mechanical drawing. Verify GPIO defaults, clock-valid timing and DSP reset release.

LVDS interface

Terminate with 100 Ω at the DSP input, allowing for internal termination. Match VOD and common mode to the receiver; VOH / VOL limits alone do not define differential swing. AC coupling requires receiver bias and recovery checks.

LVPECL interface

Provide the specified 50 Ω-to-(VDD−2 V) loading or a validated equivalent. The source needs a DC current path and the receiver needs appropriate bias. Check termination current and signal levels at supply limits.

Power and layout

Place 0.1 µF directly between VDD and GND near the device. Keep the differential pair short and symmetric over a continuous return plane. Evaluate filter drop, resonance and transients at the XO pins.

Thermal and mechanical integration: keep the XO clear of switching nodes, laser-driver current loops and steep thermal gradients. Check local temperature, pad geometry, height, reflow-induced frequency shift and board stress on the assembled module.

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08

Clock Quality, Thermal Budget & Validation

Low phase noise · ±20 ppm frequency stability · −40 to +105°C local operating range

The low phase noise of a high-fundamental quartz source must be preserved through the supply, termination and clock-distribution path. Evaluate reference noise with the DSP PLL transfer function and the actual REFCLK loading; device-only jitter does not establish module-level margin.

Typical phase noise at 312.5 MHz

Offset frequency	LVDS typical	LVPECL typical
10 kHz	−147 dBc/Hz	−135 dBc/Hz
100 kHz	−156 dBc/Hz	−154 dBc/Hz
1 MHz	−158 dBc/Hz	−160 dBc/Hz

Conditions: 3.3 V supply, 312.5 MHz carrier. These typical points are not a maximum phase-noise mask and do not reconstruct the full integration curve. Evaluate the complete spectrum, spurs and the defined 12 kHz–20 MHz jitter band.

PAM4 timing margin

Reference noise transferred through the DSP PLL consumes the transmit and sampling clock budget. Validate the complete path against the DSP mask and confirm lock, BER and FEC behavior during DSP load changes and laser operation.

±20 ppm frequency budget

At 312.5 MHz, ±20 ppm corresponds to ±6.25 kHz. Verify cold start, frequency extrema across temperature and hot steady state against the DSP input window. Define how initial error, supply variation and aging enter the total budget.

−40 to +105°C operation

Use the local XO temperature for thermal validation; module case temperature is a separate measurement. First-year aging is ±3 ppm/year at 25°C. Evaluate long-term operation against the required service life.

Module qualification and acceptance

Validation item	Required evidence
Configuration and pinout	Exact part, 312.5 MHz, supply and output; Pin 1 E/D, Pin 2 NC, Pins 4/5 OUT/OUTN.
Frequency and temperature	±20 ppm, −40 to +105°C; temperature sweep, supply limits, cold start and hot steady state.
Output compatibility	Single-ended levels, VOD, common mode, duty cycle, termination, coupling and load.
Phase noise and jitter	Full spectrum, 12 kHz–20 MHz integration, spur treatment and DSP mask / PLL weighting.
Startup and low power	Supply ramp, clock-valid time, DSP reset, disable/re-enable timing and standby state.
Module link and assembly	Lock, BER/FEC, traffic, laser operation, supply perturbation, thermal cycling, reflow and mechanical clearance.

Traceable results: associate measurements with the full ordering code, sample lot, PCB revision, instrument, frequency reference, supply, termination and temperature. Qualify each selected voltage and output configuration on the target module.

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09

Technical Resources & FCom Engineering Support

Product specifications · official platform documentation · application engineering

FCom supports optical-module solution providers with source selection, interface review and module-validation planning. Provide the following information for each external clock position so that the proposed configuration matches the receiving device and operating environment.

Platform and reference node

DSP / SerDes / FPGA / retimer model and mode; physical REFCLK input; schematic and clock tree; existing BOM; number of independent reference domains.

Electrical and timing limits

Exact frequency; supply range; LVDS / LVPECL or other accepted format; coupling, load, VOD and common mode; jitter band, phase-noise mask, spurs and PLL bandwidth.

Module integration

XO local temperature; package and maximum height; pad constraints; power and control waveforms; startup sequence; sample stage and qualification conditions.

FCom configuration review

We align frequency, supply, output, stability, temperature and control requirements to the full ordering code. Qualification records remain specific to the selected part and module design.

Product documents and platform references

FCO-6LH product specification
Electrical limits, phase noise, mechanical outline and pinout.
Product / datasheet →

FCO-2LH product specification
Electrical limits, phase noise, mechanical outline and pinout.
Product / datasheet →

Broadcom BCM83822-DIE
800G 8:4; 312.5 / 625 MHz reference.
Technical reference →

Broadcom BCM85826-DIE / BCM85812
4:4 uses 312.5 / 625 MHz; 8:8 uses 156.25 MHz.
Technical reference → · **BCM85812 →**

AMD Versal HBM VHK158
Programmable RC21008A reference clocks.
Technical reference →

Intel / Altera Agilex 7 I-Series
Network interfaces and board clock circuits.
Technical reference → · **Interfaces →**

Texas Instruments DS280DF810
Reference-free retimer architecture; verify the exact device.
Technical reference →

FCom differential oscillator portfolio
Host and module references by frequency, output and package.
Technical reference →

FCOM APPLICATION ENGINEERING

Define your optical-module clock

Share the DSP, REFCLK schematic, timing budget and module operating conditions. We will support part selection and interface evaluation.

Technical review →

Source edition: 30 October 2026. Configuration-specific guarantees follow the applicable FCom specification. Platform references describe architecture and do not imply adoption or qualification of an FCom device. All third-party names belong to their respective owners.

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