

HIGH-SPEED OPTICAL TIMING

Optical Communications & High-Speed Modules

Frequency-control solutions for high-speed optical communication systems requiring ultra-low-jitter, high-frequency and compact reference clocks across PAM4, SerDes, DSP, PHY and coherent-optical architectures.

Ultra-Low Jitter + High-Frequency Differential Clocking + PAM4 / SerDes Signal Integrity

100G / 200G / 400G

800G / 1.6T

PAM4

400ZR / 800ZR

OTN / DWDM

Optical Line Cards

Engineering Focus

Begin with the actual clock node—PHY / SerDes reference, high-frequency PLL reference, tunable clock-recovery node or module-controller clock—then select the oscillator class that matches the confirmed interface and performance requirements.

Architecture Consideration

Optical line rate does not define a single universal oscillator. Depending on the PHY / DSP architecture, the external reference may be 156.25 MHz, 312.5 / 625 MHz, or generated by an oscillator integrated within the device.

156.25 MHz

Mainstream public external REFCLK example.

312.5 / 625 MHz

200G/lane public REFCLK examples.

External / Integrated

Architecture must be confirmed first.

Jitter Budget

Validate with the receiver specification.

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Application Scope & System Architecture

Optical Communications & High-Speed Modules covers pluggable optics, optical PHY/DSP platforms and optical line systems where clock quality directly supports high-speed electrical SerDes, PAM4 signal integrity, DSP processing and architecture-specific coherent or OTN functions.

Representative Equipment

Pluggable Optical Modules

- 100G / 200G / 400G Modules
- 800G / 1.6T Modules
- QSFP / QSFP-DD / OSFP
- PAM4 Optical Links

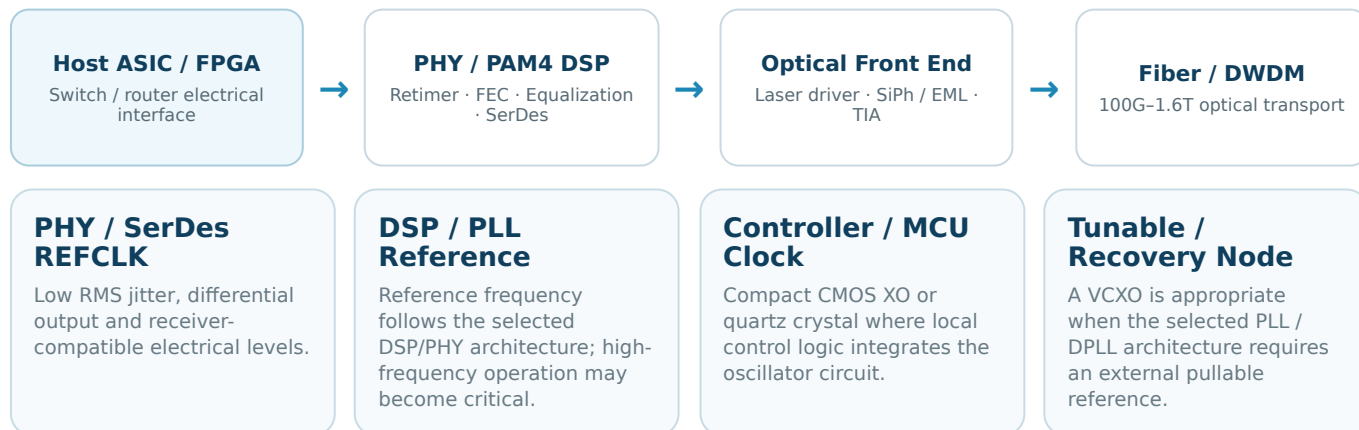
Coherent & Transport

- 400ZR / 800ZR / ZR+
- Coherent Optical Modules
- OTN / WDM / DWDM
- Data Center Interconnect

System-Level Platforms

- Optical Line Cards
- Switch / Router Optical Interfaces
- PHY / Retimer Platforms
- DSP / SerDes Subsystems

Representative Signal & Clock Domains



Architecture boundary: optical line rate does not automatically define the external oscillator frequency. Some DSPs use an external 156.25 MHz reference, some 200G/lane designs use 312.5 / 625 MHz, and some highly integrated DSPs incorporate the oscillator internally.

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Select by System Node First

Start from the actual clock node. Then confirm whether the reference is externally supplied or generated inside the DSP/PHY before selecting frequency, interface and performance class.

System Node	Typical Clock Function	Representative Frequency	Preferred FCom Direction	Selection Focus
PAM4 PHY / DSP External REFCLK	PLL / SerDes reference for 100G-800G class PHY	156.25 MHz; architecture-dependent 161.1328125 MHz	FCO-2L-UJ / FCO-3L-UJ	Use when an external differential reference falls inside the 100-220 MHz UJ range. Confirm LVDS / LVPECL / HCSL and the receiver jitter integration bandwidth.
200G/lane High-Frequency REFCLK	High-frequency PLL reference for 800G / 1.6T generation	312.5 / 625 MHz on selected public PHYs	FCO-3L-PG for evaluation	The 10-1500 MHz frequency range covers these reference clocks. Jitter is specified at 0.6 ps; confirm compliance with the receiving PLL / PHY budget before design-in.
Clock Recovery / Tunable PLL	External pullable reference where required by DPLL / CDR	Architecture-specific	FVC-3L-PG	Select this option when the PLL / DPLL requires an external VCXO and the required pull range has been defined.
Module MCU / Management	Controller, monitoring and housekeeping	Typical 25 / 50 MHz class	CMOS XO or quartz crystal	Choose by oscillator topology, package, supply and—when using a crystal—CL / ESR. Specific FCom series are selected later.
Line-Card Local PHY / FPGA	Local network / FPGA reference	100 / 125 / 156.25 MHz depending interface	CMOS or differential XO as required	Select CMOS or differential output according to the target receiver interface rather than frequency alone.

Direct Series Selection

A specific FCom series is identified when the clock requirement falls within a clearly matching frequency, interface and performance range.

Further Validation

For 312.5 / 625 MHz references, frequency coverage is available, while final suitability depends on the receiving jitter and phase-noise budget.

Supporting Clock Selection

For MCU and management clocks, select the device class first; the detailed FCom series follows from the controller oscillator topology, frequency, supply and package requirements.

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Frequency & Component Placement Matrix

Use frequency together with system position, interface and clock role. The same optical data rate can use different external references depending on the selected PHY / DSP architecture.

Frequency / Family	Typical System Position	Reference Status	Representative FCom Series	Engineering Interpretation
25 / 50 MHz	Module MCU, controller, local digital logic	Supporting	CMOS XO or quartz crystal	Use a crystal when the target IC includes the oscillator circuit and the required CL / ESR values are defined.
100 / 125 MHz	Line-card PHY / FPGA / local interface clock	Common	CMOS or differential XO	Choose output logic from the target receiver; frequency alone is not sufficient.
156.25 MHz	PAM4 PHY / SerDes / DSP external reference	Primary	FCO-2L-UJ / FCO-3L-UJ	Recommended FCom range: 100-220 MHz with 50 fs jitter. Confirm the required output logic and jitter integration bandwidth.
161.1328125 MHz	Architecture-specific Ethernet / FPGA / SerDes reference	Architecture-dependent	Ultra-low-jitter differential XO class	Within the FCom ultra-low-jitter frequency range; select the final series after confirming that the platform requires this exact external reference.
312.5 MHz	200G/lane PHY / high-frequency PLL reference	Public PHY example	FCO-3L-PG for evaluation	The frequency range supports this reference clock. Jitter is specified at 0.6 ps; confirm compliance with the receiver budget.
322.265625 MHz	FPGA / SerDes architecture-specific reference	Architecture-dependent	High-frequency differential XO class	Confirm the exact external REFCLK and jitter requirement before selecting the final FCom series.
625 MHz	Next-generation 200G/lane PHY / 800G-1.6T reference	Public PHY example	FCO-3L-PG for evaluation	The frequency range extends to 1.5 GHz. Confirm the receiving PLL jitter requirement before final selection.

Selection note: the 50 fs jitter specification applies to the published 100–220 MHz ultra-low-jitter range. For 312.5 / 625 MHz references, evaluate the high-frequency differential family and verify the receiving PHY / PLL jitter budget.

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Representative Platform & Architecture Matrix

The following public platforms illustrate representative optical clock architectures. FCom series are referenced by functional suitability only and do not imply original-platform adoption, qualification, compatibility or pin-to-pin replacement.

BROADCOM

BCM87422 · 400G PAM4 Optical PHY

1

Platform overview: 400G 4×106G PAM4 PHY for QSFP112 / SR4-class optics. Broadcom states that on-chip clock synthesis uses a **156.25 MHz external reference clock** through high-frequency, low-jitter PLLs.

Clock architecture: mainstream external-reference architecture; the external oscillator does not run at optical lane rate.

156.25 MHz REFCLK → PHY PLL / DSP → 4×106G PAM4

FCom selection direction: FCO-2L-UJ / FCO-3L-UJ are suitable for evaluation because the public platform uses a 156.25 MHz external REFCLK within their published 100–220 MHz range. Confirm output logic and jitter integration bandwidth against the PHY specification.

MAXLINEAR

MxL93683 · 800G PAM4 DSP

2

Platform overview: 800G 8×100G electrical / 8×100G optical DSP platform for QSFP-DD800 / OSFP. MaxLinear states that an **integrated crystal oscillator eliminates the need for a costly reference clock source**.

Clock architecture: high integration can remove the external high-speed XO from the primary DSP clock node.

Host 8×100G → Integrated Oscillator + DSP → Optical 8×100G

FCom selection direction: this architecture integrates the oscillator within the DSP, so the primary high-speed DSP clock does not require an external XO. Evaluate FCom devices only for separate controller or management clock nodes defined by the complete module design.

BROADCOM

BCM85826-DIE · 800G / 1.6T 200G-per-Lane PHY

3

Platform overview: four 212.5 Gb/s PAM4 lanes for 800G DR4 / 1.6T DR8-class architectures. Broadcom states that clock synthesis uses a **312.5 / 625 MHz external reference clock**.

Clock architecture: the 200G/lane generation moves the external reference into a substantially higher frequency domain.

312.5 / 625 MHz → Low-jitter PLL → 4×212.5G PAM4

FCom selection direction: FCO-3L-PG covers the 312.5 / 625 MHz frequency range and can be evaluated for this clock node. Jitter is specified at 0.6 ps; final suitability depends on the PHY reference-clock budget.

JUNIPER · COHERENT · MARVELL

PTX10002-36QDD + 800ZR + Orion Coherent DSP

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Platform overview: public 800ZR system demonstration combining Juniper PTX10002-36QDD, a Coherent 800ZR transceiver and Marvell Orion coherent DSP for IP-over-DWDM / DCI and metro applications.

Clock architecture: coherent modules add DSP, ADC/DAC and optical-carrier domains, but the publicly available platform information does **not** disclose one universal external oscillator frequency.

800GbE Host → Coherent DSP / ADC-DAC → IC-TROSA / DWDM

FCom selection direction: the publicly available platform information does not disclose one universal external REFCLK frequency. Confirm the coherent DSP clock requirement first, then select the appropriate FCom oscillator class.

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High-Speed Optical Clock Architecture

This representative architecture separates host-interface timing, DSP / PHY references, high-frequency clocking, optical conversion and local management clocks. Representative FCom series are shown where the clock requirement supports a clear engineering selection.

LAYER 1 Host / Network ASIC	Switch / Router ASIC 100G / 400G / 800G host electrical interface SerDes / C2M High-speed electrical lane interface	Supporting REFCLK When the host ASIC / FPGA uses an external reference, select the device class after confirming the actual REFCLK frequency and interface.
LAYER 2 PHY / PAM4 DSP	DSP / Retimer FEC · equalization · gearbox / retiming PLL / Clock Synthesis External or integrated reference architecture	Primary Optical Timing Node 156.25 MHz external-reference architectures provide a direct selection point. FCO-2L-UJ / FCO-3L-UJ · 100–220 MHz UJ range
LAYER 3 200G/lane REFCLK	High-Frequency REFCLK 312.5 / 625 MHz public PHY examples High-Frequency PLL Generates internal high-speed timing domains	High-Frequency Reference Evaluation 312.5 / 625 MHz reference clocks require a dedicated high-frequency differential oscillator class. FCO-3L-PG · 10–1500 MHz · 0.6 ps jitter; verify against the receiver requirement
LAYER 4 Optical Front End	TX Laser driver / SiPh / EML / modulator RX Photodiode / TIA / optical receiver	Optical Front-End Clocking A timing component is selected only when the optical subassembly exposes a defined reference-clock input.
LAYER 5 Module Management	MCU / Monitor Telemetry · configuration · housekeeping Local Oscillator Crystal or CMOS XO depending IC architecture	Compact Local Clock Choose between a CMOS XO and quartz crystal only after the controller oscillator topology, package, supply and CL / ESR requirements are known.

Reference-design note: SAW filters and MCF crystal filters are not primary components in the standard high-speed optical-module clock path. OCXO solutions are generally more appropriate to chassis-level precision timing than to compact pluggable modules.

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Device Selection by System Function

Select the oscillator architecture according to the clock function and required performance. Frequency, package and output format are finalized after the external-clock requirement and receiver budget are confirmed.

Ultra-Low-Jitter Differential XO

Recommended when an external 100–220 MHz differential reference is required for PHY / SerDes / DSP clocking.

Representative FCom: FCO-2L-UJ / FCO-3L-UJ

Key specifications: 50 fs jitter, ± 20 ppm stability, -40 to $+125^{\circ}\text{C}$, LVDS / LVPECL / HCSL.

High-Frequency Differential XO

Recommended when the required external reference exceeds the ultra-low-jitter family range, including 312.5 / 625 MHz-class nodes.

Representative FCom: FCO-3L-PG

Key specifications: 10–1500 MHz frequency range, 0.6 ps jitter. Verify the receiving PHY / PLL jitter budget before design-in.

Differential VCXO

Recommended when the selected PLL / DPLL requires an external pullable reference.

Representative FCom: FVC-3L-PG

Key specifications: 10–1500 MHz frequency range with ± 50 to ± 150 ppm pullability.

Compact Local Clock

Recommended for module MCU / management logic requiring a local clock.

Select a CMOS XO or quartz crystal according to oscillator topology, frequency, package, supply and CL / ESR requirements.

Temperature-Compensated Reference

Recommended when temperature stability is a primary requirement in addition to clock quality.

Evaluate the TCXO class against the required stability, jitter / phase-noise performance, package and power budget.

Integrated-Clock Architectures

Some DSPs integrate the primary oscillator or do not expose an external high-speed reference input.

In these architectures, select FCom components only for clock nodes that are externally accessible and electrically defined.

Application boundary: FCom SAW Filter / SAW Resonator and MCF Crystal Filter families address RF / IF signal-conditioning needs and are not universal components in digital optical modules. OCXO and tuning-fork products should be considered only where a specific chassis-level timing or housekeeping function requires them.

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Representative FCom Selection Guide

The following FCom series are highlighted where their published specifications directly support a meaningful engineering selection. Supporting local-clock products are selected after the controller architecture and electrical requirements are confirmed.

Selection Need	FCom Series / Part Family	Package	Frequency	Supply	Output	Stability / Temp.	Jitter / Phase-Noise Data	Use / Boundary
156.25 MHz / 100-220 MHz ultra-low-jitter differential REFCLK	FCO-2L-UJ / FCO-3L-UJ	2520 / 3225	100-220 MHz	1.8 / 2.5 / 3.3 V	LVPECL / LVDS / HCSL	± 20 ppm · $-40 \sim +125^{\circ}\text{C}$	50 fs	Recommended for external differential REFCLKs within this range when the receiver jitter specification is compatible.
312.5 / 625 MHz high-frequency external REFCLK	FCO-3L-PG	3225	10-1500 MHz	2.5 / 3.3 V	LVPECL / LVDS	± 25 ppm · $-40 \sim +105^{\circ}\text{C}$	0.6 ps	Recommended for evaluation at 312.5 / 625 MHz where a 0.6 ps jitter specification meets the receiving PLL / PHY requirement.
External tunable / clock-recovery reference	FVC-3L-PG	3225	10-1500 MHz	2.5 / 3.3 V	LVPECL / LVDS	± 25 to ± 50 ppm · $-40 \sim +105^{\circ}\text{C}$	PN matrix: -107 @100 Hz; -111 @1 kHz; -114 @10 kHz dBc/Hz	Recommended when the selected DPLL / CDR requires an external VCXO; pullability options are ± 50 to ± 150 ppm.
Module controller / management local clock	FCom CMOS XO / Quartz Crystal families	2016-3225 class	Controller-specific	1.8 / 2.5 / 3.3 V or passive	CMOS or crystal resonator	Application-dependent	Supporting local-clock function	Select the detailed series after confirming the MCU oscillator topology, frequency, package, supply and, for crystal designs, CL / ESR.

Ordering guidance: the application guide identifies representative series rather than a final ordering code. FCom will confirm the frequency, supply voltage, output format, stability, temperature range and applicable options before quotation or production release.

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Engineering Validation & Selection Checklist

For design-in and production release, confirm the receiving clock interface, jitter / phase-noise budget and environmental requirements before finalizing the FCom series and ordering code.

Platform & Clock Node

- 100G / 200G / 400G / 800G / 1.6T / coherent
- PHY / DSP / SerDes / PLL / MCU location
- External reference, integrated oscillator or recovered-clock architecture
- Module form factor: QSFP / QSFP-DD / OSFP / line card

Frequency & Interface

- Exact REFCLK frequency
- LVDS / LVPECL / HCSL / CMOS input requirement
- Supply voltage and enable / standby behavior
- Termination, swing and rise/fall-time limits

Jitter & Phase Noise

- Maximum RMS jitter
- **Integration bandwidth** used for the jitter specification
- Phase-noise mask at required offsets
- PLL receiver mask / reference-clock budget

Environmental & Mechanical

- Operating and case-temperature requirement
- Frequency stability over temperature
- Package / height restriction
- Power and current budget inside the optical module

VCXO-Specific Inputs

- Confirm an external VCXO is actually required
- Pull range / APR
- Control-voltage range
- Frequency and differential output format

Commercial / Qualification

- Prototype quantity and required sample date
- EVT / DVT / PVT / MP stage
- Annual volume
- Required reports, qualification and change-control expectations

Series Selection

When the external reference, output interface and jitter budget align with a published FCom range, proceed to detailed series selection.

Additional Validation

When frequency coverage is available but performance margins remain system-dependent, confirm jitter / phase noise and temperature requirements before design-in.

Integrated Clock Architecture

When the DSP integrates the primary oscillator, evaluate FCom products only for separate clock nodes defined elsewhere in the module.

Send the clock node, frequency, logic, supply, jitter bandwidth, temperature and package — FCom can narrow the series before quotation. **Technical Review →**

09

Engineering FAQ & Application Review

Is 156.25 MHz always the correct optical-module oscillator?

No. It is a very common external reference in Ethernet/PAM4 PHY architectures, but some 200G/lane platforms use 312.5 / 625 MHz and some DSPs integrate the oscillator internally. Follow the selected PHY/DSP clock input.

How should I choose between the ultra-low-jitter and high-frequency oscillator families?

Use the ultra-low-jitter family when the external differential reference falls within 100-220 MHz and jitter is the primary requirement. For higher-frequency references such as 312.5 / 625 MHz, evaluate the high-frequency family and confirm that its jitter performance meets the receiving PLL / PHY budget.

How should 312.5 / 625 MHz reference clocks be evaluated?

First confirm that the target PHY / DSP requires the external reference. Then verify output logic, supply voltage and the receiving jitter / phase-noise limits. Frequency coverage alone is not sufficient for final component selection.

When is an external VCXO appropriate?

An external VCXO is appropriate when the selected clock-recovery or PLL architecture specifically requires a pullable reference. Confirm nominal frequency, pullability and control-voltage requirements before selection.

Are SAW and MCF filters part of a standard optical-module clock solution?

Generally no. They should be used only where a real RF/IF filtering function exists. They are not universal components in digital PAM4 or coherent optical modules.

How is the final FCom ordering code determined?

The final ordering code depends on frequency, supply voltage, output format, stability, temperature range and applicable options. FCom engineering confirms these parameters during the design-in or RFQ review.

Public Architecture References

1. Broadcom BCM87422 — 400G 4×100G PAM4 PHY; public 156.25 MHz external reference clock: Broadcom BCM87422
2. MaxLinear MxL93683 — 800G PAM4 DSP; public integrated-crystal-oscillator architecture: MaxLinear MxL93683
3. Broadcom BCM85826-DIE — 800G / 1.6T 200G-per-lane PHY; public 312.5 / 625 MHz external reference clock: Broadcom BCM85826
4. Juniper / Coherent / Marvell public 800ZR demonstration: 800ZR System at OFC'24

Product data note: FCom series and specifications shown in this guide are based on the current FCom product portfolio. Final specifications and ordering details should be confirmed for the target frequency and configuration.

Discuss Your Optical Timing Requirement

Send the target platform or DSP/PHY, clock node, reference frequency, output logic, supply voltage, RMS-jitter requirement with integration bandwidth, temperature range, package and prototype / annual volume.

[General Inquiry](#)
[Technical Support](#)