

PRECISION REFERENCE & METROLOGY TIMING

Network, Frequency & Timing Analyzers

Precision measurement and metrology equipment requiring highly stable, low-noise and phase-coherent references.

Accuracy + Stability + Aging + Phase Coherence

Vector Network Analyzers

Phase-Noise / VCO Analyzers

Frequency Counters

Time-Interval Analyzers

Clock Metrology

Calibration Systems

Engineering Focus

Begin with the actual reference node—external laboratory input, internal holdover timebase, disciplined pullable source, coherent LO / synthesizer reference, or ADC / FPGA sampling clock—then match the device class to that function.

Architecture Consideration

A nominal frequency is not a complete specification. Accuracy, warm-up, aging, close-in phase noise, jitter bandwidth, pullability and channel-coherence requirements should be evaluated independently.

10 MHz

Common laboratory reference interface.

±5 ppb

Representative FCom OCXO stability class.

**–162
dBc/Hz**

FOC-5S-LN at 10 kHz offset.

50 fs

FCO-3L-UJ typical RMS jitter.

01

Application Scope & System Architecture

Network, Frequency & Timing Analyzers applications include precision instruments that compare amplitude, phase, frequency and time against a controlled reference. The timing architecture must preserve traceability while preventing the internal clock from masking the device under test.

Representative Equipment

Network & RF Measurement

- Vector network analyzers
- Scalar / component analyzers
- Coherent multi-port receivers
- Calibration and verification sets

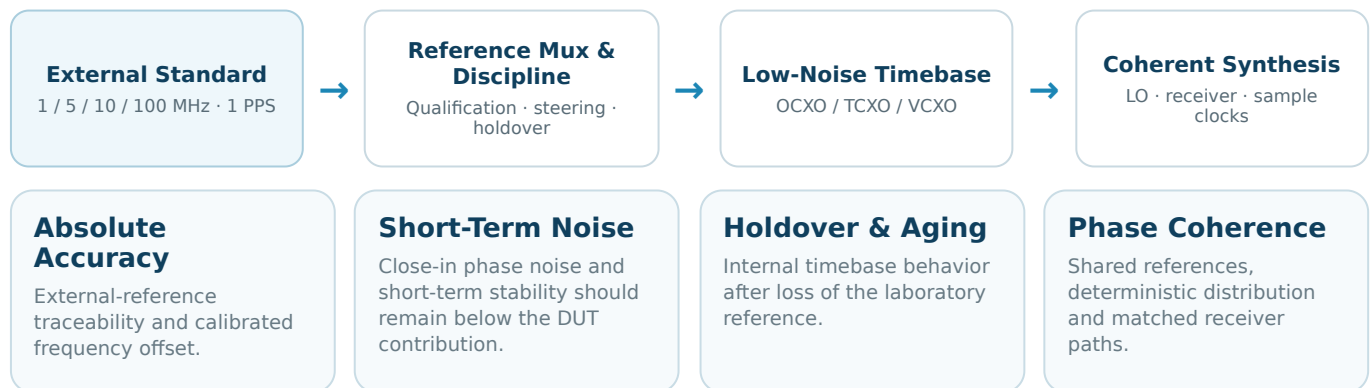
Frequency & Phase Noise

- Phase-noise / VCO analyzers
- Signal-source analyzers
- Frequency-stability analyzers
- Cross-correlation measurement

Time & Clock Metrology

- Frequency counters
- Time-interval analyzers
- Timestamping systems
- Clock / oscillator characterization

Representative Reference Chain



Architecture boundary: the oscillator alone does not guarantee instrument accuracy. Reference input qualification, PLL loop bandwidth, distribution noise, power-supply isolation, thermal control, calibration interval and firmware steering all contribute to the final metrology result.

02

Select by System Node First

Identify what the node must preserve—traceable accuracy, low close-in noise, pullable discipline or low-jitter distribution—before choosing the device class.

System Node	Typical Function	Representative Frequency	FCom Solution Direction	Selection Focus
Internal Master Timebase	Free-run and holdover reference when external standard is absent	10 MHz primary; 5 / 20 / 25 / 40 MHz possible	FOC-5S-LN when the published phase-noise floor drives selection; FOC-7S when compact 9×7 SMD placement is the deciding constraint	Warm-up, aging, retrace, close-in phase noise, supply and thermal design.
Reference Discipline / Fine Steering	PLL / DPLL corrects local timebase to an external reference	2-66 MHz CMOS; higher-frequency differential when required	FVC-3X supports defined low-frequency CMOS pullable nodes; differential VCXO selection follows confirmation of the target interface	Pull range, control voltage, loop bandwidth and phase-noise transfer.
Temperature-Stable Secondary Reference	Fast-start reference or compact instrument timebase	5-52 MHz	High-precision TCXO class; FVT-7S-WT provides a -40 to +105°C option for wider-temperature operation	Published stability to ±50 ppb; aging and absolute calibration should be confirmed separately.
ADC / FPGA Sampling Clock	Low-jitter clock for digitizers, phase detectors and processing	100 / 122.88 / 125 / 156.25 / 200 MHz	FCO-3L-UJ provides a 3225 differential option for 50 fs-class clock requirements	Logic family, termination and receiver integration bandwidth still require confirmation.
Controller / Local Logic	MCU, display, communication and housekeeping	10 / 20 / 25 / 40 / 50 MHz class	CMOS XO or quartz crystal	Keep outside the critical metrology path; select by topology, package, supply and CL / ESR.

Reference First

For a traceable timebase, prioritize stability, aging and phase noise before package size.

Loop-Aware Selection

A VCXO is appropriate when the disciplining loop and required pull range are defined.

Separate Supporting Clocks

Controller and housekeeping clocks should remain independent from the primary measurement reference.

03

Frequency & Component Placement Matrix

Use frequency to locate the system node, then complete the selection with stability, noise, tuning and output-interface requirements.

Frequency / Family	Typical System Position	Status	FCom Solution Direction	Engineering Interpretation
1 PPS	Timing epoch, trigger alignment, timestamp correlation	Interface	System-level input; no oscillator assignment	Use with a frequency reference. Edge conditioning, delay calibration and timestamp resolution dominate.
1 / 5 MHz	Legacy lab reference or divided standard	Platform-dependent	OCXO or reference-synthesizer architecture, subject to confirmation of the instrument's internal conversion scheme	Confirm whether the instrument synthesizes a 10 MHz internal master from the incoming reference.
10 MHz	External Ref In / Out; internal holdover; phase-noise analyzer reference	Primary	FOC-5S-LN may be evaluated for low-noise holdover references; FVC-3X supports defined pullable discipline nodes	Absolute accuracy, aging and phase-noise requirements should be specified separately.
20 / 25 / 30.72 / 38.88 / 40 / 50 MHz	Local synthesizer, telecom-derived reference, FPGA / converter support	Common class	OCXO for holdover, TCXO for compact stability, or XO for supporting logic	Package and series selection is finalized after stability, warm-up, output and placement requirements are confirmed.
100 / 122.88 / 125 / 156.25 / 200 MHz	High-rate reference, converter clock, coherent digital receiver or FPGA	Architecture-dependent	FCO-3L-UJ when a 3225 differential 50 fs-class clock is the actual node requirement	The range is 100–220 MHz; confirm LVPECL / LVDS / HCSL and jitter integration bandwidth.
220–1500 MHz	High-frequency PLL / LO reference or fast digital clock	Conditional	FCO-3L-PG for fixed output; FVC-3L-PG for externally pullable operation	Frequency capability alone is insufficient; published jitter or phase noise should be validated against the receiving loop.

System design note: a 10 MHz OCXO may define traceability and holdover while a separate 100–200 MHz low-jitter XO clocks the digitizer. Treating these functions as separate clock domains provides a clearer performance budget.

04

Representative Platform & Architecture Matrix

Four public instruments illustrate how reference architecture changes by measurement domain. These examples are included solely as public architecture references; FCom makes no claim regarding component adoption or internal BOM content.

KEYSIGHT TECHNOLOGIES

N5245B PNA-X Microwave Network Analyzer

1

Public architecture: 900 Hz / 10 MHz to 50 GHz PNA-X with multiple coherent sources and reference receivers. Published specifications expose 10 MHz Ref In and Ref Out for synchronization to a laboratory standard.

10 MHz Lab Ref → Coherent Sources → Test / Ref Receivers

Design takeaway: a shared low-noise reference is the phase-coherence anchor; source, LO and receiver paths still require calibrated distribution and thermal control.

ROHDE & SCHWARZ

FSWP Phase-Noise Analyzer & VCO Tester

2

Public architecture: 1 MHz to 56 GHz analysis range with dual-channel cross-correlation. Published reference inputs cover 1-50 MHz plus 100 MHz / 1 GHz; reference outputs include 1-50 MHz and 100 MHz.

DUT / Ref → Dual Channels → Cross-Correlation

Design takeaway: the internal reference and two measurement channels should remain below the DUT noise floor; close-in phase noise is more important than a generic jitter figure.

MICROCHIP

53100A Phase Noise Analyzer

3

Public architecture: independent DUT and reference inputs from 1 to 200 MHz, single- or dual-reference operation and cross-correlation processing. A 100 MHz internal-reference option supports phase-noise and stability measurements.

1-200 MHz DUT → Correlation Engine → PN / ADEV

Design takeaway: independent reference paths and correlation reduce instrument-added noise; timebase aging and reference quality remain part of the uncertainty budget.

PENDULUM INSTRUMENTS

CNT-104S Multi-Channel Frequency Analyzer

4

Public architecture: four parallel 400 MHz inputs, gap-free timestamping, 7 ps timestamp resolution and up to 20 million readings/s. External reference validation is documented at 1 / 5 / 10 MHz; Ref Out follows the active timebase.

1 / 5 / 10 MHz Ref → 4-Channel Timestamp → Statistics / ADEV

Design takeaway: timestamp resolution, channel simultaneity and a common reference determine multi-channel phase and frequency comparability.

05

10 MHz Traceable Phase-Noise & Stability Analyzer

A bench instrument accepts a laboratory reference, preserves measurement continuity with an internal low-noise timebase and uses a pullable element only inside a defined disciplining loop.

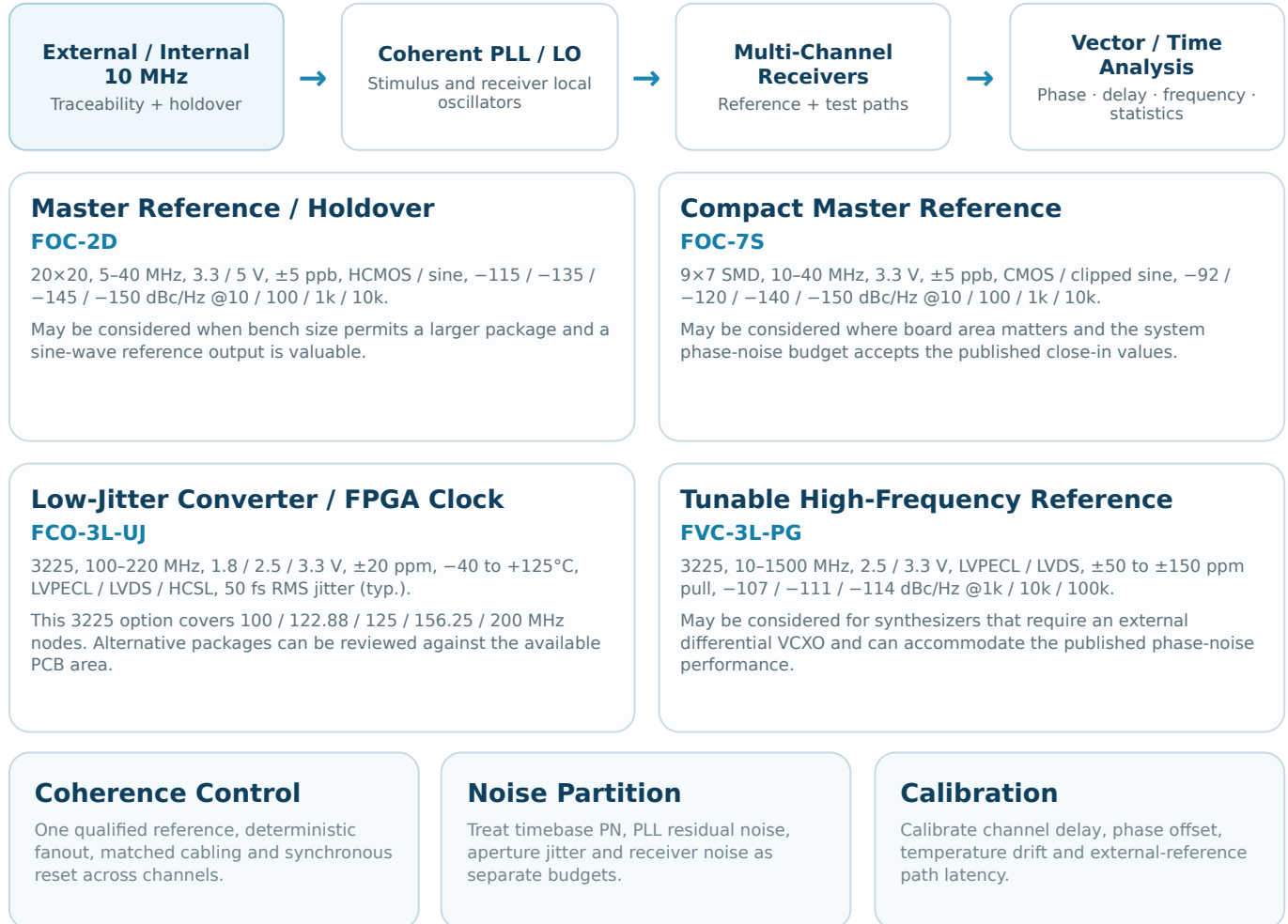
LAYER 1 Reference Inputs	10 MHz House Standard Rubidium / cesium / GNSS-disciplined source	1 PPS / Alternate Ref Epoch and redundancy input	System Interface Qualification, amplitude limiting, isolation and loss-of-reference detection.
LAYER 2 Reference Mux	Input Selection Auto / manual priority with hysteresis	Phase Detector / DPLL Slow steering loop for noise isolation	Discipline Node Use a pullable local oscillator only after loop range and bandwidth are defined. FVC-3X · 2–66 MHz · ± 50 to ± 150 ppm pull
LAYER 3 Internal Holdover	Thermally Managed Timebase Free-run during external-reference loss	10 MHz Distribution Low-noise fanout to measurement channels	Primary FCom Node Low-noise 10 MHz master option with published stability to ± 5 ppb. FOC-5S-LN · –120 / –145 / –157 / –162 dBc/Hz @10 / 100 / 1k / 10k
LAYER 4 Measurement Paths	DUT / Reference Channels Independent mixers or phase detectors	Cross-Correlation Suppress uncorrelated instrument noise	Layout Focus Matched distribution, isolated supplies, shielding, low thermal gradients and calibrated delay.
LAYER 5 Digital Analysis	ADC / Timestamp Phase records and counter data	PN / ADEV / TDEV Uncertainty-aware processing	Separate Clock Domain The converter clock complements—and does not replace—the traceable 10 MHz timebase.

Representative placement: FOC-5S-LN may be evaluated as the low-noise holdover reference, while FVC-3X supports a defined discipline loop. Final loop performance also depends on control sensitivity, bandwidth, reference noise, DAC noise and thermal design.

06

Coherent VNA / Multi-Channel Timing Architecture

A common reference is divided into a low-noise synthesis domain and a low-jitter digitizer domain so that source coherence, receiver phase and timestamp alignment can be optimized independently.



Optional RF / IF filtering: FCom MCF crystal filters (selected 7.8–60 MHz fixed-IF families) and SAW filters (110–3550 MHz coverage) may be considered where the analyzer includes a narrowband IF or RF preselection node. These filters are specified separately from the timing architecture.

07

FCom Selection Guidance

The following FCom selection anchors address six recurring design decisions in precision analyzer platforms. Additional package and supporting-clock options can be confirmed after the clock-node requirements are defined.

Low-Noise OCXO · Primary

FOC-5S-LN

Low-noise internal timebase for phase-noise and stability measurement.

Package: 14×9 6-SMD
Frequency: 10–40 MHz
Stability / Temp: ±5 ppb · –40 to +85°C
Phase noise: –120 / –145 / –157 / –162 dBc/Hz @10 / 100 / 1k / 10k

Compact OCXO

FOC-7S

Compact SMD holdover reference for space-constrained instruments.

Package: 9×7 4-SMD
Frequency: 10–40 MHz
Stability / Temp: ±5 ppb · –40 to +85°C
Output: CMOS / clipped sine

Wide-Temperature TCXO

FVT-7S-WT

High-temperature reference option for thermally demanding equipment.

Package: 7050 4-SMD
Frequency: 10–52 MHz
Stability / Temp: ±50 ppb · –40 to +105°C
Phase noise: –130 / –148 / –156 dBc/Hz @100 / 1k / 10k

CMOS VCXO

FVC-3X

Pullable local reference for disciplined 10–50 MHz-class loops.

Package: 3225 6-SMD
Frequency: 2–66 MHz
Pullability: ±50 to ±150 ppm
Output / Temp: CMOS · –40 to +105°C

Ultra-Low-Jitter XO

FCO-3L-UJ

3225 differential sampling and FPGA clock for the 100–220 MHz domain.

Supply: 1.8 / 2.5 / 3.3 V
Stability / Temp: ±20 ppm · –40 to +125°C
Output: LVPECL / LVDS / HCSL
Jitter: 50 fs

High-Frequency XO / VCXO

FCO-3L-PG / FVC-3L-PG

10–1500 MHz differential families for architecture-specific PLL / LO nodes.

Package: 3225 6-SMD
Supply: 2.5 / 3.3 V
Output: LVPECL / LVDS
Boundary: Validate 0.6 ps XO jitter or VCXO phase noise in-system

OCXO Priority

FOC-5S-LN emphasizes low phase noise; FOC-7S emphasizes compact placement. The system priority determines the preferred direction.

Fixed vs. Pullable

FCO-3L-PG supports fixed-frequency operation, while FVC-3L-PG supports an externally steered loop.

Sampling Clock Interface

FCO-3L-UJ is intended for differential 100–220 MHz nodes with a defined output interface and jitter bandwidth.

Final ordering code: FCom confirms the frequency-specific suffix after reviewing frequency, voltage, output, stability, temperature, pullability and package requirements.

08

Engineering Validation & Minimum RFQ

Convert the instrument requirement into one specification set per clock node. This prevents a supporting digital clock from being evaluated against the master timebase criteria.

Reference Interface & Topology

- Internal timebase, external Ref In / Out, 1 PPS or all three
- Exact frequency and input amplitude / impedance
- Automatic reference switching and holdover behavior
- Sine, clipped sine, CMOS, LVDS, LVPECL or HCSL

Accuracy, Stability & Aging

- Initial calibration accuracy
- Temperature stability and operating profile
- Daily / monthly / yearly aging requirement
- Warm-up time, retrace and calibration interval

Phase Noise & Jitter

- Phase-noise mask at exact offset frequencies
- Spurious limits and measurement floor target
- Maximum RMS jitter with integration bandwidth
- PLL residual noise and clock-distribution contribution

Discipline / VCXO Inputs

- Required pull range or APR
- Control-voltage range and slope
- DPLL loop bandwidth and acquisition range
- DAC resolution, noise and reference quality

Mechanical, Power & Thermal

- Package / height, SMD or DIP preference
- Supply voltage, current and warm-up power
- Ambient, airflow and thermal-gradient conditions
- Vibration, shielding and low-noise supply plan

Commercial & Qualification

- Prototype quantity and required sample date
- EVT / DVT / PVT / production stage
- Annual volume and target life cycle
- Qualification, reports and change-control expectations

Bench Validation

Measure PN, spurs, frequency offset, warm-up, sensitivity to supply and thermal airflow.

System Validation

Verify loop behavior, holdover transition, channel coherence, timestamp alignment and calibration repeatability.

Uncertainty Review

Confirm that the reference contribution remains below the DUT and instrument uncertainty targets.

Send one clock-node specification per function — FCom can narrow the series and prepare the final ordering code. [Technical Review](#) →

09

Engineering FAQ & Application Review

Why is 10 MHz so common in precision instruments?

It is a widely supported laboratory reference interface that is easy to distribute and synthesize. It does not replace the need to specify input level, lock range, noise, holdover and calibration behavior.

OCXO or TCXO for the internal timebase?

An OCXO should be considered when ppb-class stability, aging and close-in phase noise drive the measurement. A TCXO can reduce size, power and warm-up time where the uncertainty and holdover budget allow it.

Can the lowest jitter XO replace the OCXO?

Usually no. The 50 fs UJ family is optimized for high-rate sampling clocks; the OCXO addresses stability, aging and low-frequency phase-noise behavior. Many instruments need both clock domains.

When is a VCXO required?

A VCXO is appropriate when a PLL / DPLL must steer an external oscillator. Pull range, control sensitivity and loop bandwidth should be specified before selecting the VCXO family.

Where do MCF and SAW filters fit?

They apply to narrowband IF or RF preselection nodes. FCom offers selected 7.8–60 MHz MCF functions and SAW-filter coverage from 110 to 3550 MHz; these components are specified independently from the timing path.

How is the final ordering code confirmed?

FCom confirms the frequency-specific suffix from the required frequency, supply, output, stability, temperature, pullability, package and optional functions.

Public Architecture References

1. Keysight N5245B PNA-X product page and technical specifications: [keysight.com/N5245B](https://www.keysight.com/na/en/products/phase-noise-analyzers/n5245b-pna-x-product-page-and-technical-specifications) · N5244B/45B specifications
2. Rohde & Schwarz FSWP product page and specifications: R&S FSWP · FSWP specifications
3. Microchip 53100A Phase Noise Analyzer data sheet: Microchip 53100A
4. Pendulum CNT-104S product page and manual: Pendulum CNT-104S · CNT manual

FCom product information: specifications reflect the current FCom product portfolio, reviewed on 20 August 2026. Final values remain subject to confirmation of the complete ordering code.

Discuss Your Analyzer Reference Architecture

Send the instrument type, clock node, exact frequency, output, supply, phase-noise mask, jitter bandwidth, stability / aging target, temperature, package and prototype / annual volume.

[General Inquiry](#)
[Technical Support](#)