

NETWORK EQUIPMENT & SMARTNICs

Network Equipment & SmartNICs

Engineering guidance for Ethernet switches, routers, NICs, SmartNICs, DPUs and network processors across PHY, host, packet-processing, high-speed Ethernet and precision-timing clock domains.

Define the Physical Node + Preserve Link Margin + Maintain Timing Integrity

Ethernet PHY

PCIe REFCLK

100 / 125 MHz

156.25 MHz SerDes

SyncE / PTP

10 MHz / 1PPS

Application Scope

Managed switches, routers, gateways, NICs, SmartNICs, DPUs, FPGA accelerator cards, network processors and top-of-rack systems.

Selection Philosophy

Selection begins at the replaceable clock input. A PHY crystal, PCIe reference, processor SYSCLK, Ethernet SerDes clock and precision-timing source remain separate nodes even when their nominal frequencies overlap.

PHY Reference

25 MHz crystal loops and 25 / 50 MHz driven PHY or RMII clocks.

Host & PCIe

100 MHz PCIe REFCLK and separate processor / FPGA system clocks.

Ethernet & SerDes

125 MHz local domains and 156.25 MHz high-speed differential references.

Precision Timing

Optional SyncE / PTP subsystems with 10 MHz holdover and 1PPS timing.

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Application Scope & Engineering Domains

Network equipment combines passive resonator loops, driven board clocks, interface-specific differential references and optional precision-timing sources.

One board, multiple independent clock trees. A 100 MHz PCIe reference, a 100 MHz processor SYSCLK, a 125 MHz generated interface clock and a 156.25 MHz Ethernet SerDes reference may coexist without being electrically interchangeable.

Typical Equipment

Switching & Routing

Managed Ethernet Switch
Router / Gateway
Network Processor
Top-of-Rack Switch
Converged Access Node

NIC & SmartNIC Platforms

Ethernet NIC
SmartNIC / DPU
FPGA Accelerator Card
PCIe Ethernet Endpoint
Packet-Offload Adapter

High-Speed Interfaces

Copper Ethernet PHY
PCIe Host Link
SGMII / XFI / SerDes
SFP / QSFP Interface
Optional SyncE / PTP Plane

Five Engineering Domains

PHY Oscillator Loop

Passive crystal requirements: CL, ESR, drive, C0, startup and negative resistance.

Driven Board Clock

CMOS supply, logic levels, direction, duty cycle, load, startup and OE behavior.

Host / PCIe Reference

Common-clock, SRNS or SRIS topology, SSC policy, termination and generation-specific jitter.

Ethernet / SerDes

LVDS, LVPECL or HCSL swing, common mode, coupling, termination and receiver mask.

Precision Timing

SyncE / PTP DPLL reference, 10 MHz continuity, 1PPS marker and holdover budget.

Passive Crystal

Exact frequency, load capacitance, ESR, C0, drive level and oscillator-loop margin.

Output Interface

CMOS, LVDS, LVPECL or HCSL levels, termination, AC coupling and receiver bias.

Jitter & Topology

Integration band, device mask, SSC, clock ownership, PLL transfer and additive jitter.

Environment & Program

Temperature, supply noise, airflow, qualification, lifecycle and production validation.

Clock-definition note: Ethernet line rate and block-diagram frequency do not prove that a standalone oscillator is present. The physical clock pin, source direction and receiving-device specification define the replaceable timing position.

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Select by System Node First

Identify the replaceable component, clock role and receiving interface before comparing crystal or oscillator families.

System Node	Clock Role	Representative Signals / Frequencies	Typical Device	Selection Focus
Ethernet PHY Oscillator Loop	Local passive resonator	25 MHz XI / XO crystal pins	MHz quartz crystal	CL · ESR · drive · C0 · tolerance · stability · startup margin
PHY / RMII Driven Clock	Externally driven PHY or interface reference	25 / 50 MHz XI CLKIN or RMII REF_CLK	CMOS XO or documented MAC / PHY source	clock direction · VDD · VIH / VIL · duty cycle · startup · OE
Processor / FPGA System Reference	Switch ASIC, NPU, FPGA or management SYSCLK	100 / 125 MHz local board reference	CMOS or differential XO	receiver interface · common mode · termination · RMS jitter · supply noise
PCI Express Host Interface	Generation-specific host reference	100 MHz CC / SRNS / SRIS · SSC as specified	HCSL-capable XO or host-supplied clock	PCIe generation · topology · termination · SSC policy · phase-jitter mask
High-Speed Ethernet SerDes	MAC, FPGA, retimer, QSFP or transceiver REFCLK	156.25 MHz 10 / 25 / 40 / 100GbE domains	Low-jitter differential XO	LVDS / LVPECL / HCSL · swing · coupling · mask · jitter band
SyncE / PTP Timing Subsystem	DPLL reference and local holdover	10 MHz + 1PPS profile-dependent timing I/O	TCXO / OCXO plus separate timing marker	stability · aging · holdover · warm-up · waveform · DPLL behavior

1 · Confirm the Physical Node

Determine whether the receiver exposes a passive oscillator loop, driven clock input, differential reference or timing-DPLL input.

2 · Define the Interface Budget

Specify CL / ESR and drive for a crystal, or VDD, logic, termination, topology and jitter band for an active clock.

3 · Validate on the Platform

Check startup, link margin, PLL behavior, temperature, supply noise and production variation on the complete board.

Recommended sequence: System node → physical clock input → source direction → frequency → interface / load → jitter or stability budget → environment → final FCom configuration.

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Frequency & Component Placement Matrix

Frequency becomes meaningful only when it is tied to the physical clock position, source direction and receiving interface.

Frequency	Representative System Position	Applicability	Selection Interpretation
25 MHz	Ethernet PHY XI / XO or documented driven local reference	PHY Reference	May be a passive crystal or active CMOS clock. Confirm the receiver mode before selecting the product class.
50 MHz	Driven RMII REF_CLK	Interface Clock	Normally a digital clock from the MAC, PHY or oscillator; use a passive crystal only where an explicit 50 MHz oscillator loop is provided.
100 MHz	PCI Express host reference	PCIe REFCLK	Qualify the PCIe generation, CC / SRNS / SRIS topology, SSC policy, output standard, termination and phase-jitter mask.
100 MHz	Processor, switch ASIC or FPGA SYSCLK / IOPLL reference	System Reference	Treat separately from PCIe. Confirm CMOS or differential signaling, swing, common mode, load and RMS-jitter band.
125 MHz	GbE, RGMII, switch fabric or local board reference	Local / Derived	May be standalone, shared or generated by a MAC, PHY or PLL. Identify the clock owner before defining an oscillator BOM position.
156.25 MHz	High-speed Ethernet, QSFP, FPGA transceiver or retimer REFCLK	Ethernet SerDes	Use a compatible low-jitter differential source after defining LVDS / LVPECL / HCSL, termination, coupling and receiver mask.
10 MHz + 1PPS	SyncE / PTP DPLL reference, PRTC interface or holdover subsystem	Precision Timing	Select TCXO or OCXO by stability and outage-time error. Treat 1PPS as a separate timing marker, not a continuous reference.

25 / 50 MHz

PHY crystal-loop and driven RMII clock domains require different product classes.

100 MHz

PCIe REFCLK and processor SYSCLK remain separate electrical positions.

125 / 156.25

Local GbE and high-speed Ethernet SerDes reference layers.

10 MHz + 1PPS

Conditional SyncE / PTP continuity and timing-marker domain.

Platform-specific interpretation: 122.88 MHz converged-access clocks, 150 MHz DDR references and other internal fabric clocks are evaluated only when the selected board exposes a replaceable component-level source.

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Representative Platform & Architecture Matrix

Four public platforms illustrate a managed switch, network processor, PCIe Ethernet endpoint and multi-clock FPGA SmartNIC.

MICROCHIP

EVB-KSZ8563 · Managed Ethernet Switch 1

Architecture: the KSZ8563 combines a managed Layer-2+ switch, two integrated 10/100 PHY ports and a host interface in a compact evaluation platform.

Public evidence: the official board guide identifies a DSC1001CI2-025.0000 25 MHz oscillator, establishing a replaceable driven-reference position.

25 MHz Board Ref → KSZ8563 L2+ Switch → 2 × PHY / RJ45

Selection insight: qualify the documented 25 MHz external-clock input. A passive crystal applies only where a derivative design exposes a compatible XIN / XOUT oscillator loop.

NXP

Layerscape LS1046A-RDB · Router / Network Processor 2

Architecture: the platform combines 1GbE, 10GbE, PCIe and DDR around an LS1046A network-processing SoC.

Public evidence: its clock table separates 25 MHz PHY references, 100 MHz differential SYSCLK and PCIe clocks, plus selectable 100 / 156.25 MHz SerDes references.

25 / 100 MHz → LS1046A NPU / SoC → 1G / 10G SerDes

Selection insight: one board exposes multiple clock classes. The 100 MHz SYSCLK and PCIe reference remain separate nets with different interface requirements.

MICROCHIP

EVB-LAN7431-EDS · PCIe Ethernet Endpoint 3

Architecture: LAN7431 integrates a PCIe endpoint, DMA, Ethernet MAC, clock / reset management and RGMII / MII connectivity to an external PHY or switch board.

Public evidence: the evaluation board uses an external 25 MHz local reference and exposes IEEE 1588 PTP connectors.

PCIe Host → LAN7431 MAC / DMA → RGMII / External PHY

Selection insight: the 25 MHz local clock can be evaluated at component level, while the PCIe reference remains a separate host-interface clock.

INTEL / ALTERA OFS

FPGA SmartNIC N6000-PL / N6001-PL 4

Architecture: PCIe Gen4, Intel Agilex FPGA processing and QSFP Ethernet coexist with system, host, local, memory and optional precision-timing clock domains.

Public evidence: the N6001 table lists 100 MHz SYS / PCIe, 156.25 MHz QSFP, 125 / 25 MHz local and 150 MHz DDR clocks; the platform brief also documents integrated OCXO and 10 MHz / 1PPS timing.

100 MHz PCIe / SYS → Agilex FPGA / DPU → 156.25 MHz QSFP

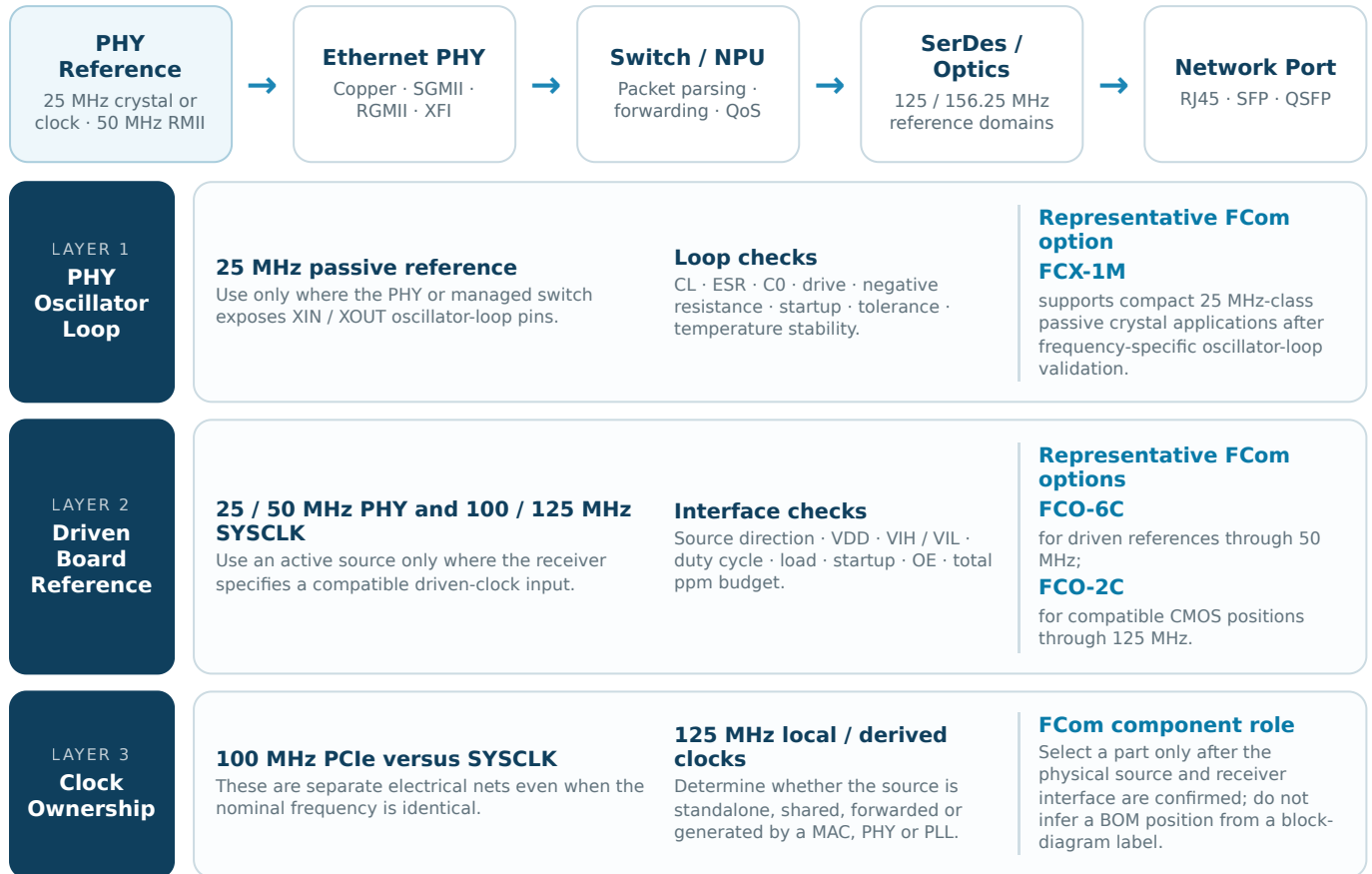
Selection insight: exposed low-jitter references and the precision source are meaningful selection nodes; DDR and internally generated clocks are not universal oscillator categories.

Platform interpretation: these public examples illustrate representative architectures only. They do not indicate FCom adoption, qualification, verified compatibility or drop-in replacement. Final selection is based on the target-device documentation, schematic and complete clock requirements.

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Switch / Router / Network-Processor Clock Architecture

Representative clock path from the local PHY reference through packet processing and high-speed Ethernet interfaces.

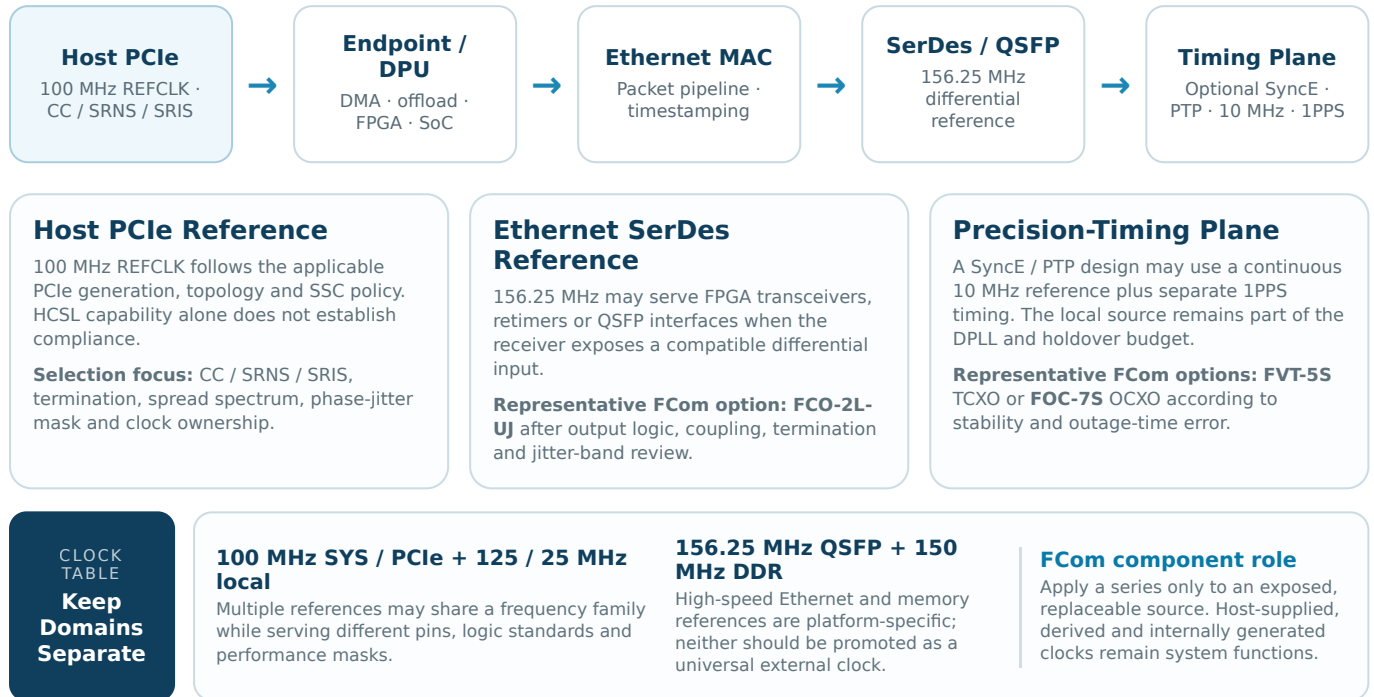


Oscillator-loop note: crystal suitability depends on the actual IC oscillator circuit, PCB capacitance and startup margin. A nominal 25 MHz match does not establish CL, ESR, drive or board-level compatibility.

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SmartNIC / DPU High-Speed & Precision-Timing Architecture

Representative path from the host PCIe clock through packet offload, Ethernet SerDes and an optional SyncE / PTP timing subsystem.



Architecture note: PCIe, Ethernet and precision timing use different metrics. Final selection follows the receiving device, interface topology, jitter or stability budget, thermal environment and complete clock-distribution path.

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FCom Selection Guidance by Design Condition

The product families below correspond to four component decisions where oscillator mode, interface or timing performance materially changes the selection.

Passive PHY Reference

Compact MHz crystal for a validated XIN / XOUT oscillator loop.

Driven CMOS Clock

PHY, RMII or board SYSCLK where the receiver accepts a digital input.

Low-jitter REFCLK

Differential PCIe / Ethernet reference selected by topology and device mask.

Precision Timing

TCXO or OCXO only where a SyncE / PTP timing plane is exposed.

Design Condition	FCom Selection	Representative Series Capability	Key Check Before RFQ
25 MHz passive PHY / switch oscillator loop	FCX-1M	1612 4-SMD crystal family covering 24-60 MHz; representative options include ± 5 ppm tolerance, ± 10 ppm stability and -40 to +125°C. CL may be 18 pF or specified; ESR is frequency-dependent, including 30-60 Ω positions.	exact IC · CL · ESR · C0 · drive · negative resistance · startup
Driven 25 / 50 MHz PHY or 100 / 125 MHz CMOS SYSCLK	FCO-6C / FCO-2C	FCO-6C: 2016 4-SMD, 1.5-50 MHz, 7-15 mA. FCO-2C: 2520 4-SMD, 1.25-125 MHz, 1.2-15 mA. Both provide 1.8 / 2.5 / 3.3 V CMOS paths with ± 20 ppm and -40 to +125°C options.	source direction · VDD · levels · load · duty cycle · startup · OE
100 / 125 / 156.25 MHz differential REFCLK	FCO-2L-UJ	2520 6-SMD, 100-220 MHz, 1.8 / 2.5 / 3.3 V, LVPECL / LVDS / HCSL, 25-65 mA, ± 20 ppm and -40 to +125°C. A 50 fs family jitter value is reviewed with its carrier, integration band, load and measurement method.	output logic · topology · termination · jitter band · device mask
10 MHz SyncE / PTP reference or holdover source	FVT-5S / FOC-7S	FVT-5S: 5032, 10-52 MHz, ± 0.5 ppm, -40 to +85°C, clipped sine / CMOS; phase noise -115 / -135 / -148 dBc/Hz at 100 Hz / 1 kHz / 10 kHz and VCTCXO pull ± 5 ppm. FOC-7S: 9 × 7 mm, 10-40 MHz, 3.3 V, ± 5 ppb, -40 to +85°C, CMOS / clipped sine; -92 / -120 / -140 / -150 dBc/Hz at 10 Hz / 100 Hz / 1 kHz / 10 kHz.	timing profile · waveform · aging · holdover · warm-up · power · DPLL

Application boundary: source-synchronous RGMII clocks, host-supplied PCIe clocks, 1PPS markers, DDR references and internally generated fabric clocks are reviewed against the actual platform before a standalone oscillator is specified. Crystal Filter and SAW products address separate RF / IF functions and are not standard elements of these board-clock paths.

ENGINEERING SELECTION SUPPORT

Request an FCom Network-Clock Recommendation

Provide the clock-tree diagram, target PHY / switch / NPU / FPGA / NIC / SmartNIC / DPU, physical clock node, frequency, interface, jitter or stability budget, temperature and project stage.

[Start Engineering Review →](#)



Engineering Validation & Minimum RFQ

Network-equipment clock selection is defined by the physical node, source direction, receiving interface and performance budget in addition to frequency.

Platform & Functional Node

- Exact PHY, switch, NPU, FPGA, NIC, SmartNIC, DPU or clock-device P/N
- Crystal loop, RMII input, SYSCLK, PCIe REFCLK, SerDes reference or timing source
- Board / module integration boundary
- Schematic, clock tree, reference BOM and revision

Passive Crystal Interface

- Frequency, CL, ESR, C0 and drive level
- IC pin capacitance and PCB stray estimate
- Tolerance, temperature stability and aging
- Negative resistance and startup margin
- Package and qualification requirement

Active Clock Interface

- CMOS / LVDS / LVPECL / HCSL
- Supply, swing, common mode and termination
- AC coupling, receiver bias, load and duty cycle
- OE / standby, startup and power sequencing
- PCIe topology and SSC policy

Performance, Environment & Program

- RMS jitter / integration band or phase-noise mask
- Stability, aging, holdover and warm-up if required
- Operating temperature and supply-noise environment
- Samples, validation plan and production schedule
- Annual volume, lifecycle and compliance scope

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Ethernet PHY crystal loop, driven PHY / RMII clock, processor / FPGA SYSCLK, PCIe REFCLK, Ethernet SerDes reference or SyncE / PTP source.
Target Device	Exact receiving IC / module part number, clock pin, schematic location, block diagram and current reference BOM.
Frequency & Topology	Physical input frequency, source direction, local / shared / forwarded / generated status, fan-out path, PCIe topology and SSC policy.
Crystal Requirements	CL, ESR, C0, drive, mode, tolerance, stability, aging, negative resistance, startup margin and package.
Oscillator Requirements	VDD, output logic, swing, common mode, termination, load, OE, RMS jitter / integration band, phase-noise mask and pull range if required.
Environment & Program	Operating temperature, supply-noise conditions, qualification, prototype quantity, sample date, annual volume, lifecycle and production location.

Crystal Validation

Measure startup, drive, frequency error, pulling and oscillator margin on the actual PHY or switch PCB across voltage and temperature.

Clock Validation

Measure phase noise, integrated jitter, spurs, amplitude, common mode, duty cycle, startup and supply sensitivity at the receiver.

System Validation

Verify PCIe / Ethernet link margin, error counters, SyncE / PTP behavior and restart performance across traffic, voltage and temperature.

Frequency alone does not define the final part: the receiver mode, source direction, electrical interface, topology, jitter or stability budget and environmental profile determine the appropriate FCom series and exact configuration.

09

Engineering FAQ & Application Review

Common network-clock questions, representative public references and the information required for FCom engineering review.

Is an Ethernet line rate the oscillator frequency?

No. A PHY or SerDes multiplies a lower reference to the serial line rate. Select from the physical crystal or clock input in the device clock tree.

Are all 100 MHz clocks interchangeable?

No. PCIe REFCLK, processor SYSCLK and distributed 100 MHz clocks can use different signaling, topology, termination and jitter masks.

Can a 50 MHz crystal drive RMII REF_CLK?

Normally no. RMII REF_CLK is a driven digital clock unless the target device explicitly implements a compatible 50 MHz crystal loop.

Is 125 MHz always a standalone oscillator?

No. RGMII and local fabric clocks may be generated by the MAC, PHY or PLL. Confirm that a component-level source is exposed.

Does an HCSL-capable XO automatically satisfy PCIe?

No. PCIe generation, CC / SRNS / SRIS topology, SSC policy, termination and phase-jitter mask must be verified together.

When should a TCXO or OCXO be used?

Only for an exposed precision-timing plane. Select the grade from the stability, aging, outage-time error, warm-up, power and DPLL requirements.

When are crystal or SAW filters considered?

Only where the system exposes a defined RF or IF filter position. They are not standard elements of these board-clock paths.

Are the listed FCom series complete ordering codes?

No. Final ordering codes depend on frequency, supply, output, stability, temperature, load and qualification.

Representative Public Technical References

1. **Microchip:** EVB-KSZ8563 official page and board user guide - managed switch architecture and 25 MHz board reference.
2. **NXP:** LS1046A-RDB official page and getting-started guide - PHY, SYSCLK, PCIe and SerDes references.
3. **Microchip:** EVB-LAN7431-EDS official page and board user guide - PCIe Ethernet endpoint, 25 MHz local reference and PTP connector context.
4. **Microchip / TI:** KSZ8081 datasheet and Ethernet PHY clocking note - 25 MHz oscillator loop versus driven 50 MHz RMII reference.
5. **Intel / Altera:** FPGA SmartNIC N6000-PL / N6001-PL product brief - PCIe, QSFP and precision-timing context.
6. **OFS:** N6001 FIM Technical Reference Manual - public external-clock table for SYS, PCIe, QSFP, DDR and local domains.
7. **Microchip:** LAN7430 / LAN7431 datasheet - local 25 MHz reference modes and RGMII / MII operating context.

FCom product specification note: product information in this guide is presented at series or representative-configuration level. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

Network Equipment & SmartNICs Review

Provide the selected platform, physical clock node, target PHY / switch / NPU / FPGA / NIC / SmartNIC / DPU, frequency, interface, topology, jitter or stability target, operating temperature and project stage. FCom application engineering can review the requirement and recommend a suitable series and configuration for system-level validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.