

SPECTRALLY CLEAN FREQUENCY REFERENCES

Low-Phase-Noise Oscillators

VCXO, TCXO, and OCXO solutions for PLLs, RF synthesis, telecom synchronization, clock recovery, and precision measurement.

- Voltage-Controlled Clock Recovery
- Temperature-Compensated & Oven-Controlled References



Start with the Required Noise Mask

Define the carrier frequency and the critical offset range before comparing products. Close-in noise, far-out noise, integrated jitter, and spurs affect different parts of the system budget.

Select by Clock Function

Use VCXO where electrical tuning is required, TCXO where temperature compensation and lower power are priorities, and OCXO where close-in noise and reference stability dominate.

FVC-3X · 2–66 MHz

1.2 ps RMS

Integrated jitter, typ. · 12 kHz–20 MHz*

FVC-5X · 1.5–170 MHz

1.0 ps RMS

Integrated jitter, typ. · 12 kHz–20 MHz*

FVT-9S-LN · 40–150 MHz

≈–160 dBc/Hz

Far-out phase noise @ 1 MHz offset, typ.*

FOC-5S-LN · 10–40 MHz

–162 dBc/Hz

Phase noise @ 10 kHz offset, typ.*

Representative series-level values are shown for preliminary selection. The metrics apply to different series and test conditions and are not directly comparable. Confirm the controlled datasheet for the exact configuration, typical/maximum status, and measurement conditions.

VCXO

Tunable Low-Noise Reference

For PLL acquisition, tracking, jitter-cleaning, and clock-recovery loops that require a controlled pull range.

FVC-3X · FVC-5X

Low-Noise TCXO

Temperature-Compensated Reference

For RF-adjacent and synchronization nodes requiring temperature compensation, lower power consumption, and no oven warm-up.

FVT-9S-LN

Low-Noise OCXO

Fixed Master Reference

For close-in-noise-sensitive synthesizers, precision timebases, and fixed reference architectures.

FOC-5S-LN

01

Select the Right Low-Noise Reference

Use the series-level portfolio to build a shortlist, then confirm the complete noise mask and controlled datasheet for the exact orderable configuration.

Phase noise is not a single-number specification. Evaluate the carrier frequency, offset points, discrete spurs, output/load, supply noise, temperature, and whether the value is typical or guaranteed.

**4 FEATURED SERIES
3 CLOCK FUNCTIONS**

VCXO — Voltage-Controlled Crystal Oscillators

CMOS · Tunable references for PLL and clock-recovery loops



FVC-3X

3.2 × 2.5 mm · 6-SMD

2–66 MHz · 2.8 / 3.3 V · CMOS
±150 ppm pull range, min. · 1.2 ps
 RMS jitter, typ. · 12 kHz–20 MHz*
 –40 to +85°C



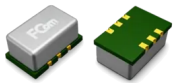
FVC-5X

5.0 × 3.2 mm · 6-SMD

1.5–170 MHz · 3.3 V · CMOS
±50 ppm APR · 1.0 ps RMS jitter, typ. ·
 12 kHz–20 MHz*
 –40 to +85°C; +105°C option by review

TCXO — Temperature-Compensated Low-Noise Reference

Low-noise fixed reference · Sine and CMOS configurations



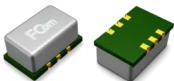
FVT-9S-LN

14.0 × 9.0 mm · SMD

40–150 MHz · low-phase-noise TCXO
±4.6 ppm total stability* · –40 to +85°C
 Sine (+8 dBm into 50 Ω) and CMOS output configurations · approx. –160 dBc/Hz @ 1 MHz offset, typ.*

OCXO — Oven-Controlled Low-Noise Reference

Fixed-frequency reference · Warm-up and thermal behavior apply



FOC-5S-LN

14.7 × 9.6 × 8.2 mm · 6-SMD

10–40 MHz · 3.3 V; 5 V option · configuration-dependent output
±10 ppb frequency stability* · –40 to +85°C
 Phase noise, typ.: –145 dBc/Hz @ 100 Hz, –157 dBc/Hz @ 1 kHz, and –162 dBc/Hz @ 10 kHz offset*

Noise Mask

Specify carrier, offsets, spurs, noise floor, and typical/maximum limits.

Integrated Jitter

State integration band, output, load, supply, and nominal frequency.

Tuning Range

Distinguish pull range from APR and define the control-voltage window.

Reference Stability

Separate temperature stability from initial tolerance, aging, and total error.

*** Performance conditions:** Marked values are series-level references for preliminary selection. Confirm typical/maximum status, carrier, supply, output/load, temperature, integration band, and test method in the controlled datasheet.

Selection guidance: Begin with clock function and package; confirm final selection against the complete electrical, environmental, and noise requirements.

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Place Spectral Purity Where It Creates System Value

Select the reference by its function in the signal chain and by the offset region that limits system performance.

System Requirement

EVM, BER, reciprocal mixing, timing jitter, or measurement floor

Noise Mask

Carrier, close-in and far-out offsets, integrated band, and spurs

Clock Architecture

VCXO, TCXO, or OCXO selected by function

System Validation

PLL interaction, power integrity, thermal behavior, and compliance

RF & Microwave Synthesis

Role: Reference into a PLL, frequency synthesizer, or coherent RF distribution chain.

Focus: Close-in noise, far-out floor, reference multiplication, discrete spurs, and supply-noise sensitivity.

FOC-5S-LN for a fixed master reference · FVT-9S-LN for a temperature-compensated RF reference

PLL, Clock Recovery & Synchronization

Role: Voltage-controlled element in acquisition, tracking, and jitter-cleaning loops.

Focus: APR/pull range, tuning sensitivity, control-voltage noise, loop bandwidth, and integrated jitter.

FVC-3X for compact loops · FVC-5X for wider-frequency requirements

Telecom, GNSS & Satcom Timing

Role: Board-level reference, timing-card reference, or synthesizer input in a disciplined architecture.

Focus: Stability budget, phase-noise multiplication, output interface, holdover requirement where applicable, and environment.

FVT-9S-LN · FOC-5S-LN; final clock-class compliance is verified at system level

Test, Measurement, Radar & RF Sensing

Role: Instrument timebase, analyzer or generator reference, radar synthesizer reference, or precision RF clock.

Focus: Measurement floor, repeatability, aging, warm-up, retrace, spurs, and calibration interval.

FOC-5S-LN as the fixed low-noise starting point · select the exact configuration against the system noise mask

Close-In Noise

Often dominates narrow-loop PLLs, coherent systems, and near-carrier modulation. Review 10 Hz to 1 kHz offsets together with drift and environment.

Far-Out Noise & Jitter

Often drives broadband clock quality and SerDes/PHY margin. Always state the integration band and the output/load condition.

Spurs & Power Integrity

A low noise floor does not guarantee a clean spectrum. Validate reference spurs, VDD coupling, VCTRL noise, and board-level grounding.

Application & Qualification Review

The applications above indicate suitable starting points. FCom confirms telecom, aerospace, automotive, or mission-critical requirements against the exact configuration and project documentation.

Validate the Complete Signal Chain

Final performance depends on the oscillator configuration, PLL transfer function, power distribution, output loading, thermal profile, and system verification plan.

03

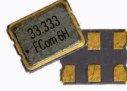
Shortlist by Clock Function

The four featured series cover tunable, temperature-compensated, and oven-controlled reference roles. Final selection follows the complete noise mask and operating conditions.

Compact VCXO

FVC-3X

2–66 MHz · VCXO



Compact CMOS voltage-controlled reference for clock recovery and synchronization loops.

3.2 × 2.5 mm

6-SMD package

±150 ppm min.

Pull range

1.2 ps RMS typ.

Jitter · 12 kHz–20 MHz*

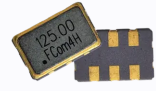
2.8 / 3.3 V

Supply options

Wide-Frequency VCXO

FVC-5X

1.5–170 MHz · VCXO



5.0 × 3.2 mm CMOS VCXO for wider-frequency PLL, broadband, and clock-recovery designs.

5.0 × 3.2 mm

6-SMD package

±50 ppm

APR reference

1.0 ps RMS typ.

Jitter · 12 kHz–20 MHz*

3.3 V

Supply

Low-Noise TCXO

FVT-9S-LN

40–150 MHz · TCXO



Temperature-compensated low-noise reference for telecom, GNSS, satcom, and RF-adjacent timing nodes.

14.0 × 9.0 mm

SMD package

±4.6 ppm

Total stability*

Sine / CMOS

Output configurations

–40 to +85°C

Operating range

Low-Noise OCXO

FOC-5S-LN

10–40 MHz · OCXO



Fixed master-reference starting point where close-in phase noise and frequency stability dominate.

14.7 × 9.6 mm

6-SMD package

±10 ppb

Frequency stability*

3.3 V / 5 V option

Supply

Configuration review

Output and test conditions

Minimum RFQ Information

Clock function

PLL/clock recovery, board reference, master reference, or instrument timebase.

Nominal frequency

Exact carrier and allowable frequency tolerance.

Noise requirement

Phase-noise mask, offsets, spurs, and jitter integration band.

Electrical interface

Supply, output, load, VCTRL, and APR/pull range.

Stability budget

Temperature, initial tolerance, aging, and warm-up where applicable.

Environment

Temperature, airflow, shock, vibration, and qualification needs.

FCom Engineering Review Can Confirm

Available Configurations

Orderable frequencies, outputs, supplies, and tuning options.

Noise & Jitter Conditions

Carrier, offsets, output/load, supply, temperature, and typical/maximum status.

PLL Compatibility

APR, pull range, tuning sensitivity, VCTRL window, and loop interaction.

Time-Domain Behavior

Integrated jitter, aging, warm-up, retrace, and holdover where applicable.

Mechanical Fit

Package, height, land pattern, and assembly requirements.

Documentation

Controlled datasheet, test data, and qualification records, as applicable.

FCOM ENGINEERING SUPPORT

Request a Low-Phase-Noise Reference Review

Share the system node, carrier frequency, required noise mask, clock function, and operating conditions. FCom will help identify the candidate series and verification path.

* Series-level reference values. Confirm the controlled datasheet for the exact configuration, typical/maximum status, and test conditions.

GENERAL INQUIRY

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TECHNICAL SUPPORT

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PRODUCT
INFORMATION