

LOW JITTER SERIES

Low-Jitter Clock Oscillators

Low-jitter reference clock solutions for high-speed digital, optical networking, data conversion, and communications systems.

Fixed-Frequency XO · Differential & CMOS Outputs · Temperature-Compensated Clocks · Tunable References

FPGA & SerDes

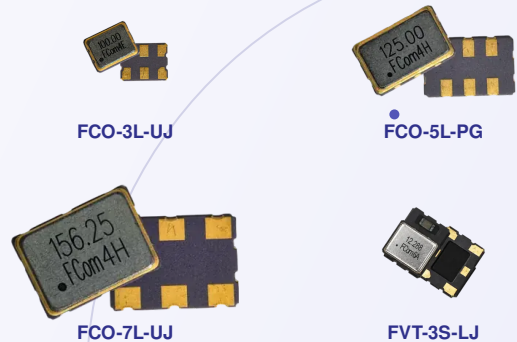
Optical Modules

Ethernet & SmartNICs

Data Converters

Telecom Equipment

High-Speed Digital



Portfolio Overview

FCom offers low-jitter XO, TCXO, and VCXO families for fixed-frequency, temperature-compensated, and voltage-controlled clock functions, with LVPECL, LVDS, HCSL, and CMOS output options.

How to Select

Begin with the clock role and jitter budget. Then match the integration bandwidth, output interface, carrier frequency, stability, temperature, supply, and package to the application.

50 fs typ.

RMS phase jitter available from selected UJ differential families, integrated from 12 kHz to 20 MHz

12 kHz–20 MHz

Integration bandwidth applied to all jitter values shown in this flyer

10–1500 MHz

Series-level frequency coverage for designated PG families; configuration dependent

+125°C

Operating temperature options up to +125°C for selected UJ families

Differential XO

Fixed Reference Clocking

Ultra-low-jitter, balanced differential, and wide-frequency families for clock distribution and high-speed interfaces.

FCO-2L/3L/5L/7L · UJ and PG variants

CMOS XO

Single-Ended Clocking

Low-jitter CMOS clocking for processors, controllers, and digital subsystems that do not require differential signaling.

FCO-3P-UJ

TCXO / VCXO

Compensated or Tunable

Temperature-compensated and voltage-controlled solutions for systems requiring enhanced stability or electrical frequency control.

FVT-3S-LJ · FVC-3L/5L/7L-PG

01

Choose the Right Clock Architecture

Use the portfolio data to establish an initial shortlist, then verify the exact orderable configuration against the latest controlled datasheet.

Select the clock as a complete electrical specification—not by the lowest jitter figure alone. Match the carrier frequency, output logic, supply, temperature, stability, package, and electrical load to the receiver and system clock budget.

Fixed-Frequency Clock Oscillators						All values: typ. RMS phase jitter · 12 kHz–20 MHz
Series / Family	Package	Frequency	Supply	Output	Stability / Temp.	Jitter typ.
FCO-2L-UJ / FCO-3L-UJ / FCO-5L-UJ	2.5 × 2.0 / 3.2 × 2.5 / 5.0 × 3.2 mm · 6-SMD	100–220 MHz	1.8 / 2.5 / 3.3 V	LVPECL, LVDS, HCSL	±20 ppm -40 to +125°C	50 fs
FCO-7L-UJ	7.0 × 5.0 mm · 6-SMD	70–170 MHz	2.5 / 3.3 V	LVPECL	±25 ppm -40 to +85°C	100 fs
FCO-2L / FCO-3L / FCO-5L / FCO-7L	2.5 × 2.0 / 3.2 × 2.5 / 5.0 × 3.2 / 7.0 × 5.0 mm	13.5–220 MHz	1.8 / 2.5 / 3.3 V	LVPECL, LVDS, HCSL	±25 ppm -40 to +105°C	150 fs
FCO-3L-PG / FCO-5L-PG / FCO-7L-PG	3.2 × 2.5 / 5.0 × 3.2 / 7.0 × 5.0 mm · 6-SMD	10–1500 MHz*	2.5 / 3.3 V	LVPECL, LVDS	±25 ppm -40 to +105°C	600 fs
FCO-3P-UJ	3.2 × 2.5 mm · 6-SMD	10–250 MHz	2.5 / 3.3 V	CMOS	±25 ppm -40 to +105°C	800 fs

Compensated & Tunable Clock Options						Phase-noise and pullability limits depend on the selected configuration
Series / Family	Clock Function	Package	Frequency	Supply	Output	Primary Selection Item
FVT-3S-LJ	Low-jitter TCXO	3.2 × 2.5 mm · 6-SMD	10–1500 MHz*	2.5 / 3.3 V	LVPECL, LVDS, CMOS	±1 ppm stability option; phase noise varies by configuration
FVC-3L-PG	Differential VCXO	3.2 × 2.5 mm · 6-SMD	10–1500 MHz*	2.5 / 3.3 V	LVPECL, LVDS	Pullability options from ±50 to ±150 ppm*
FVC-5L-PG / FVC-7L-PG	Differential VCXO	5.0 × 3.2 / 7.0 × 5.0 mm · 6-SMD	10–1500 MHz*	2.5 / 3.3 V	LVPECL, LVDS	±50 ppm APR; select the control range by application

- 1 · Set the jitter budget

Use UJ families for the tightest integrated phase-jitter requirements.
- 2 · Match the interface

Align LVPECL, LVDS, HCSL, or CMOS with the receiver and termination.
- 3 · Define clock control

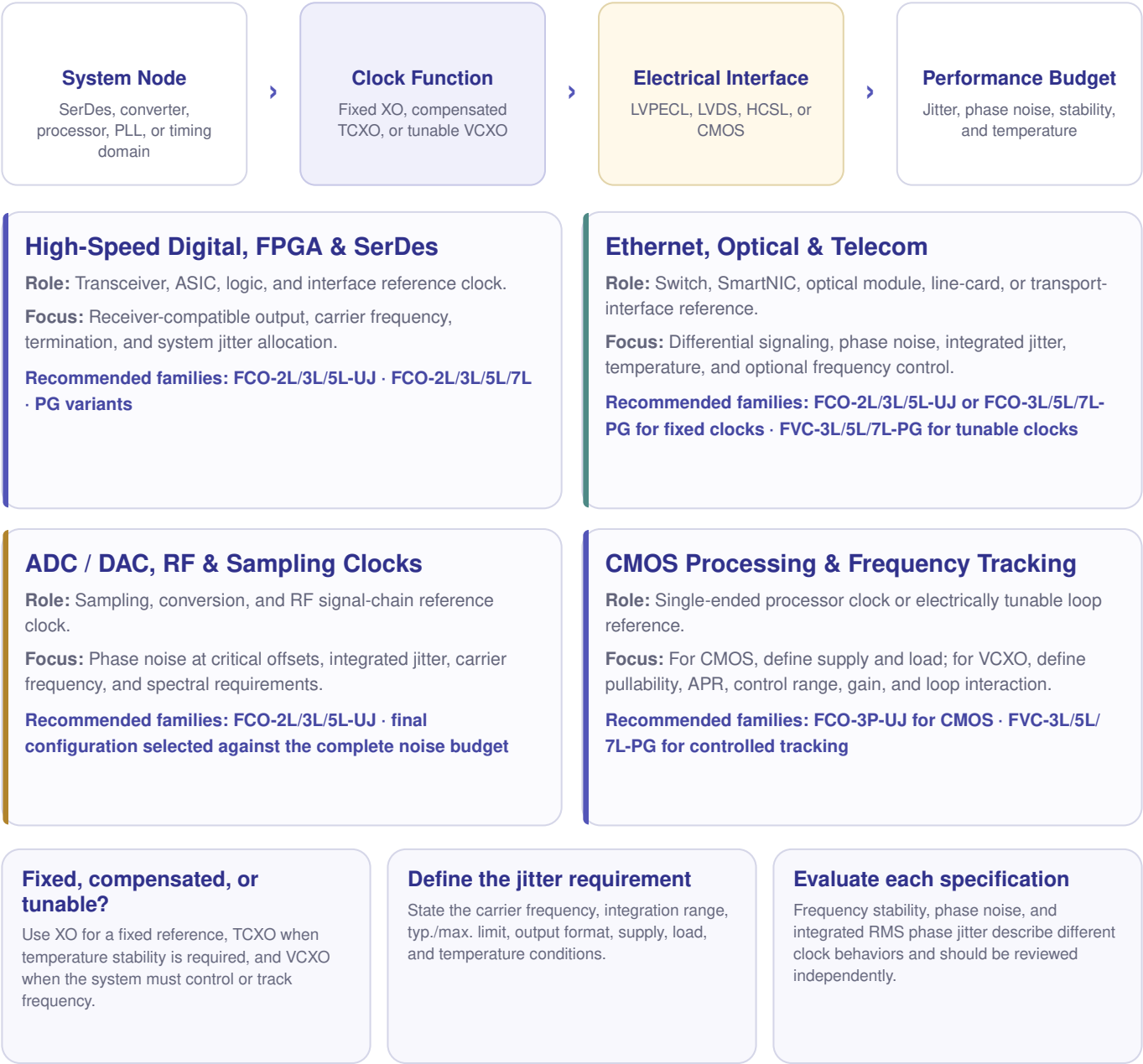
Select XO for fixed, TCXO for compensated, or VCXO for tunable clocking.

Performance qualification: All jitter values in this flyer are typical RMS phase jitter integrated from 12 kHz to 20 MHz. For design release, verify the carrier frequency, output, supply, load, temperature, and exact orderable configuration. *Frequency coverage and pullability are configuration dependent.

02

Select by System Node First

Identify the clock function and receiver interface before comparing oscillator families and series-level performance data.



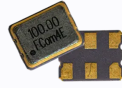
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Shortlist by Clock Role and Jitter Budget

The featured series below provide practical selection references. The final orderable part number is defined by the complete electrical, mechanical, noise, and environmental requirements.

Ultra-Low-Jitter XO

FCO-3L-UJ


50 fs

 typ. RMS
12 kHz–20 MHz

Compact differential XO for applications with stringent integrated phase-jitter budgets.

3.2 × 2.5 mm

6-SMD package

100–220 MHz

Frequency range

LVPECL / LVDS / HCSL

Output options

-40 to +125°C

Operating range

Differential XO

FCO-3L


150 fs

 typ. RMS
12 kHz–20 MHz

Balanced differential XO for high-speed clock distribution and interface reference functions.

3.2 × 2.5 mm

6-SMD package

13.5–220 MHz

Frequency range

1.8 / 2.5 / 3.3 V

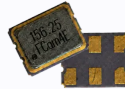
Supply options

-40 to +105°C

Operating range

Low-Jitter CMOS XO

FCO-3P-UJ


800 fs

 typ. RMS
12 kHz–20 MHz

Single-ended CMOS XO for processors, controllers, and digital subsystems.

3.2 × 2.5 mm

6-SMD package

10–250 MHz

Frequency range

CMOS

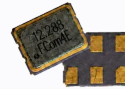
Output format

2.5 / 3.3 V

Supply options

Differential VCXO

FVC-3L-PG


VCXO

 frequency & pullability
vary by configuration

Tunable differential VCXO for PLL, frequency-tracking, and controlled-reference functions.

3.2 × 2.5 mm

6-SMD package

10–1500 MHz

Frequency range

LVPECL / LVDS

Output options

±50 to ±150 ppm

Pullability options

Information Required for Review

Clock function

Fixed XO, temperature-compensated TCXO, or tunable VCXO.

Frequency & output

Exact frequency, LVPECL/LVDS/HCSL/CMOS, and termination.

Noise requirements

Jitter limit and integration range; phase-noise offsets where applicable.

Electrical conditions

Supply voltage, receiver load, enable logic, and control voltage.

Stability & environment

Stability target, operating temperature, and aging requirement.

Project requirements

Package, height, annual usage, schedule, and documentation.

FCom Engineering Review

Output-Interface Coverage

LVPECL, LVDS, HCSL, and CMOS options across the portfolio.

Application-Led Selection

Series selection based on the clock role, receiver interface, and system jitter budget.

Jitter & Phase Noise

Carrier frequency, offsets, integration band, output, supply, load, and measurement setup.

Stability Definition

Initial tolerance, temperature, supply, load, and aging terms.

VCXO Control

Pullability, APR, control range, and tuning behavior.

Configuration Confirmation

Orderable options, package, land pattern, test data, and documentation.

TALK TO FCOM

Request a Low-Jitter Clock Review

Share the clock role, frequency, output, supply, jitter or phase-noise limits, stability, temperature, and package constraints. FCom will review the requirements, recommend suitable series, and define the verification conditions for the selected configuration.

GENERAL INQUIRY

FCom@fujicrystal.com

TECHNICAL SUPPORT

support@fujicrystal.com

