

INDUSTRIAL ETHERNET & COMMUNICATION

Industrial Ethernet & Communication

Provide stable reference clocks for Ethernet PHYs, switches, gateways and FPGAs, supporting reliable links, deterministic communication and high-speed network interfaces.

PHY Reference + Switch / MAC + Gateway + FPGA / SerDes + Deterministic Network Timing

Ethernet PHY

EtherCAT

PROFINET

EtherNet/IP

TSN / PTP

FPGA / SerDes

Application Scope

Industrial Ethernet PHYs, EtherCAT controllers, managed switches, gateways, network processors, FPGA-based communication modules and high-speed SerDes interfaces.

Selection Philosophy

Selection begins with the receiving network clock node. A 25 MHz PHY crystal, 50 MHz RMII clock, 125 MHz Gigabit reference and 156.25 MHz SerDes REFCLK serve different functions within the network clock architecture.

PHY Reference

Local crystal, XO or shared PHY reference.

Switch / MAC

RMII / RGMII and Gigabit network clock domains.

Gateway

Host and dedicated network-processing domains.

FPGA / SerDes

Low-jitter high-speed differential REFCLK.

01

Application Scope & Engineering Domains

Industrial network platforms combine PHY, switch, processing, high-speed interface and synchronization clocks with different source and signal requirements.

One network, multiple reference classes. Ethernet data rate and protocol cycle time do not directly define the external crystal or oscillator frequency. The receiving PHY, switch, network processor or FPGA clock input establishes the timing requirement.

Typical Equipment

Industrial Ethernet

10/100 Ethernet PHY
Gigabit Ethernet PHY
Managed Ethernet Switch
TSN Switch
EtherCAT Slave / ESC

Communication Platforms

PROFINET Device
EtherNet/IP Adapter
Modbus TCP Gateway
Protocol Converter
Industrial Edge Gateway

High-Speed Network

FPGA Ethernet Interface
Industrial PC / Edge Compute
SFP / SFP+ Interface
SerDes / Backplane
PCIe-connected Network Logic

Five Engineering Domains

Ethernet PHY Timing

XTAL / CLKIN reference and
PHY clock output.

Switch & MAC Timing

RMII / RGMII / Gigabit network
timing.

Gateway & Network Processor

Host and dedicated
communication-processor
domains.

FPGA / SerDes Timing

100 / 125 / 156.25 MHz high-
speed REFCLK.

Deterministic Synchronization

PTP / TSN / SyncE and
precision-reference extensions.

Clock Interface

XTAL pins · CMOS CLKIN ·
shared / forwarded clock ·
differential REFCLK.

Crystal Parameters

CL · ESR · drive level ·
startup margin · temperature.

Driven Clock Parameters

VDD · logic · load · OE ·
RMS jitter · termination.

Network Architecture

Local source · PHY output ·
clock sharing · fan-out ·
clock generator.

Clock-definition note: 100 Mbps / 1 Gbps / 10 Gbps data rate, EtherCAT cycle time, TSN gate schedule, RGMII / SGMII line rate and FPGA fabric frequency are distinct from the external reference clock.

02

Select by System Node First

Begin with the receiving clock interface, then evaluate frequency, source topology, device class and electrical performance.

System Node	Clock Role	Representative External Reference	Typical Device	Selection Focus
10/100 Ethernet PHY	PHY oscillator reference	25 MHz	Crystal / XO	XTAL vs CLKIN · CL / ESR · accuracy · drive
RMII PHY / MAC	Interface REF_CLK	50 MHz	Forwarded clock / CMOS XO	clock direction · source · load · sharing
EtherCAT ESC	ESC / PHY reference	25 MHz common	Crystal / XO	shared clock · CLK25OUT · ppm · loading
Gigabit PHY / MAC	Network reference	25 / 125 MHz class	Crystal / XO	topology · local vs forwarded source · jitter
Ethernet Switch	Switch / MAC clock tree	25 / 50 / 125 MHz	CMOS XO / clock distribution	fan-out · VDD · logic · source architecture
Gateway / Network Processor	Protocol / processing reference	20 / 24 / 25 / 40 / 48 MHz class	Crystal / CMOS XO	IC-specific oscillator input
FPGA / PCIe Logic	Logic / transceiver reference	100 / 125 MHz	CMOS / differential XO	jitter · logic · termination
SerDes / SFP+	High-speed REFCLK	156.25 MHz	Low-jitter differential XO	LVDS / LVPECL / HCSL · RMS jitter · SI
PTP / TSN / SyncE	Precision synchronization reference	Architecture-dependent	XO / TCXO / OCXO	accuracy · holdover · phase noise · system timing budget

1 · Identify the Receiver

Start from the PHY, ESC, switch, network processor, FPGA or SerDes device together with the clock pins used in the design.

2 · Establish Clock Topology

Establish whether the reference is local, shared, forwarded, generated by a PHY or supplied by a dedicated oscillator.

3 · Apply Electrical Requirements

For crystals, evaluate CL / ESR / drive; for driven clocks, evaluate VDD / logic / jitter / termination and distribution load.

Recommended sequence: System node → clock direction / topology → external reference frequency → crystal or driven clock → jitter / accuracy → temperature → package → final FCom configuration.

03

Frequency & Component Placement Matrix

Industrial Ethernet references progress from local PHY oscillators to driven MAC clocks and high-speed differential SerDes REFCLKs.

Frequency	Representative System Position	Applicability	Selection Interpretation
20 / 24 MHz	Gateway / network processor / communication MCU	Platform-Dependent	Follows the selected processor oscillator input; not an Ethernet line-rate reference.
25 MHz	Ethernet PHY / EtherCAT ESC / shared PHY clock	Common External Reference	Core Industrial Ethernet reference; local crystal, external XO and shared-clock architectures should be evaluated according to the target PHY / ESC interface.
40 / 48 MHz	Gateway / communication controller / USB-related processing	Platform-Dependent	Controller-specific reference rather than a universal Ethernet clock.
50 MHz	RMII REF_CLK / driven PHY-MAC interface	Interface-Dependent / Often Forwarded	May be generated by a PHY from 25 MHz or supplied by a local XO, depending on RMII topology.
100 MHz	FPGA / PCIe / high-speed network logic	High-Speed Extension	Driven reference where output logic and jitter become primary selection parameters.
125 MHz	Gigabit Ethernet / MAC / switch / FPGA	High-Speed Network Reference	May be local, forwarded or generated within a network clock tree.
156.25 MHz	SerDes / SFP+ / high-speed Ethernet / FPGA transceiver	High-Speed Differential Reference	Typically calls for a low-jitter differential oscillator matched to the receiver interface.

25 MHz
PHY / EtherCAT core external reference.

50 MHz
RMII driven or forwarded interface clock.

125 MHz
Gigabit MAC / switch / FPGA network reference.

156.25 MHz
SerDes / SFP+ differential low-jitter REFCLK.

Reference clock ≠ data rate: 100 Mbps Ethernet does not imply a 100 MHz oscillator; 1 Gbps does not imply a 1 GHz oscillator; 10 Gbps does not imply a 10 GHz oscillator. The external reference is defined by the receiving IC clock architecture.

04

Representative Platform & Architecture Matrix

Four public platforms illustrate PHY clock conversion, shared EtherCAT reference distribution, dedicated TSN network processing and high-speed FPGA / SerDes timing.

MICROCHIP

KSZ8081RNA · 25 MHz PHY Reference → 50 MHz RMII

1

Architecture: a 25 MHz crystal or reference feeds the Ethernet PHY; the RNA configuration can provide a 50 MHz RMII REF_CLK to the MAC, while other variants can accept an external 50 MHz RMII clock.

Public evidence: Microchip documents the 25 MHz crystal / oscillator and RMII clock-direction options for the KSZ8081 family.

25 MHz XTAL / XO → Ethernet PHY → 50 MHz RMII

Selection insight: a 50 MHz RMII interface may use a locally driven clock or a PHY-generated reference, depending on the clock-source direction and system architecture.

BECKHOFF

ET1100 · EtherCAT ESC + Shared 25 MHz Clock

2

Architecture: 25 MHz crystal or oscillator feeds the EtherCAT Slave Controller; crystal-based designs can use CLK25OUT to provide 25 MHz to Ethernet PHYs, while oscillator-based designs can share one source across ESC and PHYs.

Public evidence: Beckhoff specifies a 25 MHz external reference with 25 ppm or better initial accuracy and publishes clock-sharing examples.

25 MHz XTAL / XO → ET1100 ESC → PHY Clock

Selection insight: crystal-based and oscillator-based implementations lead to different loading, fan-out and clock-distribution considerations.

RENESAS

YCONNECT-IT-RZN2L · Industrial Ethernet / TSN Network Processor

3

Architecture: host application processor connects to RZ/N2L as a dedicated network-processing domain with Industrial Ethernet functions, Gigabit switching and PHY connections.

Public evidence: RZ/N2L integrates a TSN-compliant 3-port Gigabit Ethernet switch and EtherCAT Slave Controller; the evaluation platform supports EtherCAT, EtherNet/IP, Modbus and dual Gigabit Industrial Ethernet.

Host CPU → RZ/N2L → GbE / TSN PHYs

Selection insight: host-processing timing and network-processing timing may reside in separate clock domains and can therefore require independent reference-clock evaluation.

AMD

VEK280 · FPGA / SerDes High-Speed REFCLK

4

Architecture: the public board clock tree includes Ethernet, FPGA transceiver and zSFP+ / HSDP reference domains.

Public clock evidence: AMD publishes 25 MHz Ethernet, 100 MHz transceiver and 156.25 MHz LVDS zSFP+ / HSDP clocks; the fixed 156.25 MHz source is described as a very-low-jitter LVDS oscillator.

25 MHz Ethernet → 100 MHz FPGA → 156.25 MHz SerDes

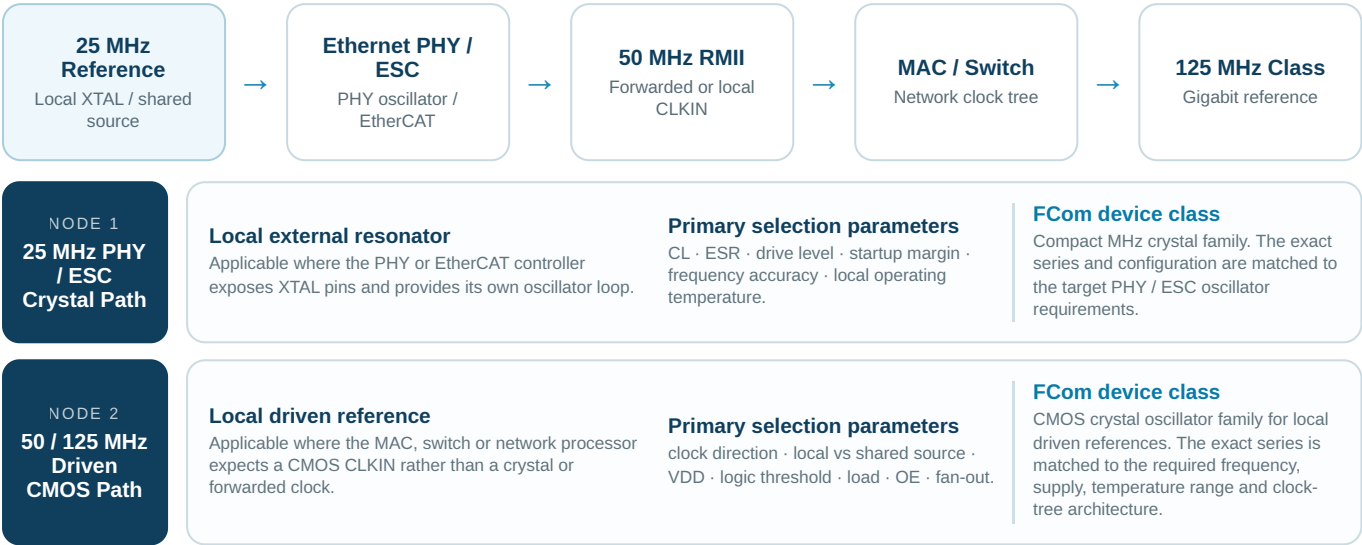
Selection insight: high-speed transceiver interfaces shift the timing focus from crystal CL / ESR toward output logic, RMS jitter and signal integrity.

Platform interpretation: these public examples illustrate representative timing architectures only. They do not indicate FCom adoption, qualification, compatibility or drop-in replacement. Final selection is based on the target-device documentation, schematic and complete system requirements.

05

Ethernet PHY + Switch / Gateway Timing Architecture

Representative timing from the local PHY oscillator through RMII / MAC and into a Gigabit switch or gateway clock tree.

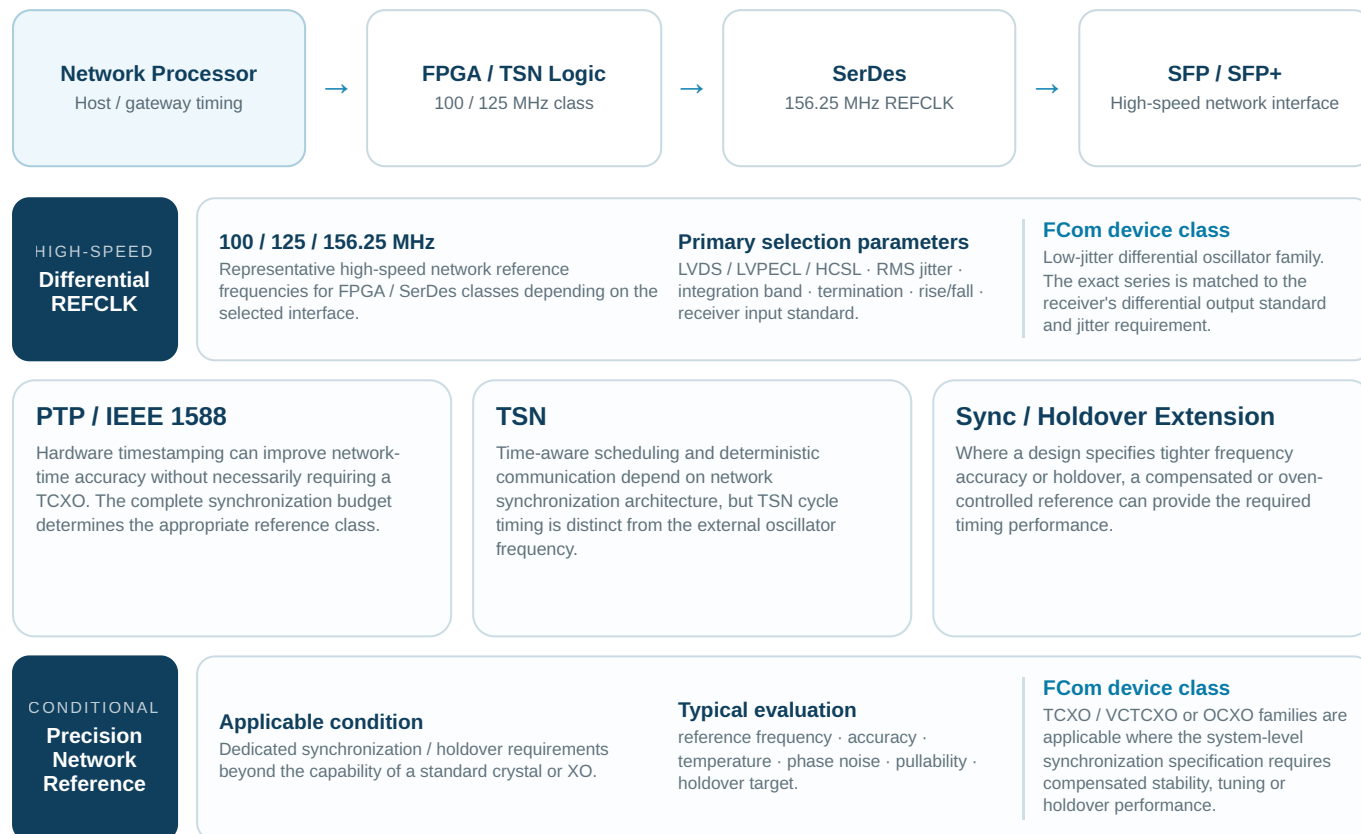


Architecture note: shared 25 MHz and forwarded 50 / 125 MHz clocks can eliminate the need for a local oscillator at the receiving node. Clock direction and distribution topology therefore determine which timing-device class is appropriate.

06

FPGA / SerDes + Deterministic Network Timing Architecture

High-speed network interfaces introduce low-jitter differential REFCLK requirements, while precision synchronization remains an application-specific timing layer.



Architecture note: precision synchronization is a separate system requirement from ordinary Ethernet link timing. Standard PHY / switch clocks are normally served by crystal or XO references, while compensated references are considered where the system-level time / frequency specification requires them.

07

FCom Selection Guidance by Design Condition

The FCom series below correspond to the principal clock-interface decisions in Industrial Ethernet and communication systems. Additional product families are considered where the application introduces specific timing requirements.

PHY / ESC XTAL

25 MHz and related local resonator references.

Driven CMOS Clock

50 / 125 MHz local CLKIN when not forwarded.

Low-Jitter Differential

100 / 125 / 156.25 MHz FPGA / SerDes REFCLK.

Precision Sync

Conditional extension only when specified by the system timing budget.

Design Condition	FCom Selection	Why It Changes the Decision	Key Check Before RFQ
PHY / ESC exposes XTAL pins	FCX-2S	The receiving IC uses its own oscillator loop, so CL, ESR, drive and startup margin define the crystal selection.	Frequency · CL · ESR · drive · temperature · package
MAC / switch / PHY expects local CMOS CLKIN	FCO-2C	The clock node requires a dedicated driven source rather than a local crystal or forwarded reference.	Frequency · VDD · logic threshold · load · OE · fan-out
100–220 MHz + differential + explicit low jitter	FCO-2L-UJ	High-speed FPGA / SerDes interfaces are selected by output standard, RMS jitter and signal-integrity requirements.	LVDS / LVPECL / HCSL · jitter band · termination · VDD

Application-specific extensions: TCXO / VCTCXO / OCXO can be evaluated when the system defines precision synchronization, holdover or tighter frequency-accuracy requirements; programmable XO can support frequency programmability or BOM flexibility; spread-spectrum clocking can support defined EMI-management architectures. VCXO, Crystal Filter, SAW Resonator and SAW Filter products address separate tuning or IF / RF functions and are evaluated independently of the core Ethernet reference-clock path.

ENGINEERING SELECTION SUPPORT

Request an FCom Industrial Ethernet Timing Recommendation

Provide the target PHY / ESC / switch / network processor / FPGA part number, clock pins, frequency, clock direction, CL / ESR or VDD / output, jitter requirement, temperature, package and project stage.

[Start Engineering Review →](#)

08

Engineering Validation & Minimum RFQ

Reliable network-clock selection considers the receiving interface, clock direction and distribution topology together with frequency.

Ethernet PHY / EtherCAT ESC

- Exact PHY / ESC part number
- XTAL pins or CLKIN
- 25 MHz local / shared reference
- CL / ESR / drive / ppm
- PHY clock-output function
- Operating temperature

RMII / RGMII / MAC

- Interface mode
- REF_CLK source / sink direction
- 50 / 125 MHz topology
- Local XO vs forwarded clock
- VDD / load / fan-out
- OE / clock sharing

Switch / Gateway / Network Processor

- Exact IC part number
- Port / PHY architecture
- Clock-tree diagram
- Reference frequencies
- Local or centralized clocking
- EMI / temperature / lifecycle constraints

FPGA / SerDes / Synchronization

- FPGA / transceiver part number
- REFCLK frequency
- LVDS / LVPECL / HCSL
- RMS jitter integration band
- Termination / load
- PTP / TSN / SyncE / holdover target if applicable

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Ethernet PHY, EtherCAT ESC, switch, gateway, network processor, FPGA, SerDes or precision synchronization node.
Target Device	Exact receiving IC part number and clock pin / schematic location.
Clock Topology	External resonator, local XO, shared source, PHY-forwarded clock, clock generator or differential REFCLK.
Crystal Requirements	Frequency, package, CL, ESR, drive level, tolerance / stability and operating temperature.
XO Requirements	Frequency, VDD, output logic, stability, RMS jitter / integration band, load, OE and termination.
Program Requirements	Prototype quantity, sample date, validation plan, annual volume, lifecycle and compliance documentation.

25 MHz Has Multiple Source Paths

Local crystal, local XO and shared ESC / PHY clocking all use the same nominal frequency but require different components.

50 MHz RMII Is Directional

The PHY may source REF_CLK to the MAC, or the PHY / MAC may receive an external clock depending on device configuration.

156.25 MHz Is a Different Device Class

High-speed differential REFCLK selection is driven by jitter and interface standard rather than crystal load parameters.

Frequency alone does not define the final part: the clock source, direction, interface type and distribution architecture determine the appropriate FCom timing series and exact configuration.

09

Engineering FAQ & Application Review

Common Industrial Ethernet timing questions and representative public architecture references.

Does 100 Mbps Ethernet require a 100 MHz oscillator?

No. Ethernet data rate and the external PHY reference are different parts of the clock architecture; many 10/100 PHYs use a 25 MHz reference.

Is 50 MHz RMII always supplied by a local oscillator?

No. Depending on the PHY / MAC configuration, 50 MHz can be generated by the PHY, supplied externally or shared from another clock source.

Why is 25 MHz common in Industrial Ethernet?

Many Ethernet PHY and EtherCAT-controller oscillator circuits use a 25 MHz crystal or oscillator reference.

Does every EtherCAT PHY need its own crystal?

No. Some ESC architectures can distribute a shared 25 MHz reference to associated PHYs.

Does Gigabit Ethernet always require a 125 MHz XO?

No. A 125 MHz reference can be local, forwarded or generated within the PHY / MAC / switch clock tree.

When is 156.25 MHz used?

It is commonly associated with high-speed Ethernet, FPGA transceivers, SerDes and SFP+ reference-clock domains.

When does jitter become a primary selection parameter?

Jitter becomes increasingly important for FPGA, PCIe, high-speed Ethernet and differential SerDes REFCLK interfaces.

When is a TCXO / OCXO relevant?

These classes are applicable when the system defines precision synchronization, holdover or reference-accuracy requirements beyond a standard crystal / XO path.

Representative Public Technical References

1. **Microchip:** KSZ8081 family — Ethernet PHY architecture with 25 MHz reference and RMII clock options.
2. **Beckhoff:** ET1100 Hardware Description — 25 MHz crystal / oscillator and CLK25OUT clock-distribution architecture.
3. **Renesas:** RZ/N2L — Industrial Ethernet processor with TSN-compliant Gigabit Ethernet switch and EtherCAT ESC.
4. **Renesas:** YCONNECT-IT-RZN2L — Industrial Ethernet / TSN network-processor evaluation platform.
5. **AMD:** VEK280 Clock Generation — public Ethernet, transceiver and 156.25 MHz high-speed reference domains.
6. **AMD:** VEK280 Fixed HSDP REF Clock — 156.25 MHz very-low-jitter LVDS reference.

FCom product specification note: product information in this guide is presented at series or representative-configuration level based on the current FCom product matrix. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable product specification and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

Industrial Ethernet & Communication Timing Review

Provide the target PHY / ESC / switch / network processor / FPGA / SerDes part number, clock input, source direction, frequency, CL / ESR or supply / output, jitter target, temperature, package and project stage. FCom can review the architecture and recommend an appropriate timing series and configuration for system evaluation and validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, with validation performed on the complete board and system.