

HIGH-SPEED DATA CONVERSION, FPGA & SERDES

High-Speed Data Conversion, FPGA & SerDes

Low-jitter reference-clock guidance for high-speed ADC / DAC platforms, RF sampling, deterministic JESD204 links, FPGA / DSP processing and multi-gigabit SerDes interfaces.

Reference Source + Jitter Cleaner + Converter Clock + SYSREF + FPGA / SerDes

High-Speed ADC / DAC

RF Sampling

JESD204B / C

FPGA / DSP

SerDes / MGT

Data Acquisition

Test & Measurement

Application Scope

Direct-RF and IF sampling, waveform generation, instrumentation, phased-array processing, software-defined radio, high-speed acquisition and FPGA-based signal-processing platforms.

Selection Approach

Start with the physical source entering the clock tree. Converter sample rate, JESD lane rate and FPGA fabric frequency do not automatically define an oscillator frequency.

Precision Reference

10 MHz laboratory references, system masters and low-noise timing sources.

Converter Clock Tree

XO / VCXO input, jitter cleaner, clock generator, sample clock and SYSREF.

FPGA / DSP

System reference, RFSoc tile clocking and deterministic JESD204 processing.

SerDes / MGT

Exact-rate differential references for high-speed serial interfaces.

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Application Scope & Engineering Domains

High-speed conversion platforms combine absolute-frequency control, low integrated jitter, deterministic timing and serial-link clocking in one system.

One platform, several clock roles. A 10 MHz master reference, 125 MHz clock-tree input, 156.25 MHz FPGA reference, generated 1 GHz sample clock and SYSREF edge may coexist without being interchangeable.

Typical Equipment

RF & Data Conversion

RF-Sampling Receiver
High-Speed ADC / DAC Board
Wideband Transceiver
Digital Beamformer
Software-Defined Radio

Acquisition & Instrumentation

Digitizer / AWG
Oscilloscope Platform
Spectrum / Signal Analyzer
ATE / Measurement System
Multi-Channel DAQ

Programmable Processing

FPGA / DSP Card
RFSoc Platform
JESD204B / C Link
SerDes Test Platform
Edge Signal Processor

Four Engineering Domains

Source / Master

Free-run accuracy, close-in phase noise, warm-up and external-reference behavior.

Clock Conditioning

PLL bandwidth, VCXO pull range, additive jitter, fan-out and power-supply isolation.

ADC / DAC

Aperture-jitter budget, input-frequency sensitivity and clock-amplitude requirements.

JESD / SerDes

Device clock, SYSREF, deterministic latency and transceiver reference masks.

Physical Source

Crystal resonator in an oscillator loop, fixed XO, VCXO, TCXO, OCXO or external input.

Output Interface

CMOS, LVDS, LVPECL, HCSL, clipped sine or sine wave.

Noise Metric

RMS integration band, phase-noise profile and receiver-specific mask.

System Environment

Temperature, airflow, vibration, power noise, startup and lifecycle.

Generated-frequency boundary: multi-gigahertz ADC / DAC clocks and JESD lane rates are commonly produced by PLLs, clock generators or converter silicon. They do not imply a discrete oscillator requirement unless the production schematic exposes a direct external-clock input.

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Select by System Node First

Classify the receiving pin and source topology before comparing frequency, jitter or package.

System Node	Clock Role	Representative Frequency	Typical Device Class	Selection Route	Selection Focus
System / Laboratory Reference	Master accuracy and close-in noise	10 MHz	TCXO or OCXO	Choose by stability, noise and warm-up	Output waveform · phase noise · holdover · power
Auxiliary Board Clock	USB, display, processor or housekeeping reference	26 / 27 / 33.33 MHz	Crystal or CMOS XO	Confirm passive loop versus driven input	CL / ESR or VDD / load · exact decimal rate
Clock-Tree Input	Reference into jitter cleaner / generator	100 / 122.88 / 125 MHz	Low-jitter XO or VCXO	Match the IC input interface and loop mode	Logic · pull range · close-in noise · RMS band
JESD / FPGA Reference	Device clock, FPGA reference or PLL input	153.6 / 156.25 / 160 MHz	Low-jitter differential XO / VCXO	Qualify against the receiver mask	LVDS / LVPECL / HCSL · termination · jitter
RFSoc / Direct Reference	External tile or converter reference	245.76 / 260 / 300 MHz	High-frequency differential XO	Distinguish fixed from programmable sources	Phase-noise profile · input amplitude · PLL mode
MGT / CPRI / SerDes	Exact-rate transceiver-bank reference	307.2 / 312.5 / 368.64 / 380.16 MHz	High-frequency differential XO / VCXO	Use the frequency-specific receiver mask	Exact rate · output swing · jitter · lifecycle
High-Frequency Reference	Direct FPGA / SerDes input where documented	491.52 / 500 / 625 MHz	High-frequency differential source	Confirm a discrete physical source exists	Receiver mask · integration band · supply noise
Converter Sample / Serial Lane	PLL- or silicon-generated operating domain	1 GHz to multi-GHz	Generated clock domain	Review the documented upstream reference	Budget the complete clock path and converter aperture jitter

1 · Identify the Physical Input

Record the exact ADC, DAC, clock IC, FPGA, RFSoc or SerDes reference pin.

Start from the schematic node, not the sample or lane rate.

2 · Classify the Source

Determine fixed XO, tunable VCXO, temperature-compensated TCXO, OCXO or generated output.

The source class defines the relevant specifications.

3 · Close the Noise Budget

Apply the receiver mask, RMS integration band, output interface and complete PLL transfer function.

A single headline jitter value is not a complete qualification.

Recommended sequence: receiving node → source topology → exact frequency → output logic → jitter / phase-noise requirement → tuning / stability → voltage → temperature → package → lifecycle.

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Frequency & Component Placement Matrix

The same nominal frequency can represent a master reference, PLL input, FPGA reference or generated output; placement determines the correct component class.

Frequency	Typical Physical Node	Source Topology	Indicative FCom Series	Engineering Boundary
10 MHz	Laboratory input, clock-module master, PLL1 reference	TCXO, OCXO or external source	FVT precision TCXO or FOC low-noise OCXO	Stability, warm-up and close-in phase noise solve different problems from integrated jitter.
26 / 27 / 33.33 MHz	Processor, USB, display and auxiliary board domains	Crystal loop or CMOS XO	FCX crystal or FCO CMOS source after topology confirmation	Exact decimal rate and receiver architecture must be preserved.
100 MHz	AD9081-class clock-tree input, FPGA system reference	CMOS or differential XO	FCO-6P-PJ for CMOS; FCO-2L-UJ for compatible differential inputs, subject to receiver review	Output interface and jitter band determine which path applies.
122.88 / 125 MHz	JESD204 clock tree, SDR reference, DAQ board source	Fixed XO or pullable VCXO	FCO-2L-UJ when differential; FVC series when loop tuning is required	Fixed and pullable sources are not interchangeable inside a PLL loop.
153.6 / 156.25 / 160 MHz	FPGA MGT, CPRI, Ethernet and PLL reference	Low-jitter differential XO / VCXO	FCO-2L-UJ for fixed 100–220 MHz differential nodes	Match the exact rate, output standard and receiver mask.
245.76 / 260 / 300 MHz	RFSoc external reference, RF-ADC clock-tree input, programmable-logic clock	High-frequency differential source	FCO-3L-PG fixed reference, subject to phase-noise review	Use as a reference input only when its full noise profile meets the system budget.
307.2 / 312.5 / 368.64 / 380.16 MHz	CPRI, MGT and high-speed SerDes reference	Fixed or tunable differential source	FCO-3L-PG or FVC-3L-PG, topology dependent	Frequency range does not establish compliance with a transceiver mask.
491.52 / 500 / 625 MHz	Direct high-frequency reference where exposed	Differential XO / VCXO or clock-generator output	FCO / FVC subject to receiver-level review	Confirm that the production platform provides a discrete source position at this frequency.
1 GHz to multi-GHz	ADC / DAC sample clock and serial lane domains	PLL, multiplier or converter-generated	Upstream FCom reference, where applicable	Qualify the upstream reference and complete clock-tree additive noise.

10 MHz

Precision master and low-noise reference.

100–160 MHz

Common converter / FPGA reference range.

245.76–380.16 MHz

RFSoc, CPRI and SerDes exact-rate references.

Generated multi-GHz

Typically generated within the system clock tree; confirm whether a discrete source is present.

Selection rule: oscillator frequency coverage is an initial screening criterion. Receiver input standard, PLL mode, phase-noise transfer, RMS integration band and deterministic-latency architecture remain part of final qualification.

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Representative Platform & Architecture Matrix

Four public platforms illustrate where a discrete physical reference source is present and where clocks are generated within the platform clock tree.

AMD

ZCU111 RFSoc Evaluation Board

01

Public architecture: Zynq UltraScale+ RFSoc with an LMK04208 / LMX2594 RF converter clock tree, programmable logic clocking and GTY transceiver references.

Published sources: 300 MHz PL user LVDS oscillator and 156.25 MHz MGT LVDS oscillator; additional 26 / 27 / 33.33 / 100 / 125 MHz board domains serve different functions.

Indicative FCom selection: FCO-2L-UJ may be considered for a fixed 156.25 MHz differential source; FCO-3L-PG may be evaluated at 300 MHz where programmability is not required. These mappings do not indicate AMD approval or AVL status.

156.25 / 300 → RFSoc / GTY → RF Data Path

ADI

AD-FMCDQA2-EBZ + FPGA Carrier

02

Public architecture: dual 1 GSPS ADC, dual 2.8 GSPS DAC and JESD204 links connect through the FMC interface to an FPGA carrier.

Published clock tree: a 125 MHz on-board source feeds AD9523-1, which generates 1 GHz ADC / DAC clocks, a 500 MHz FPGA reference and SYSREF.

Indicative FCom selection: the upstream 125 MHz source is the relevant discrete-source selection point. FCO-6P-PJ may be considered where a CMOS input is confirmed; FCO-2L-UJ applies only where the production input is documented as differential. The 500 MHz and 1 GHz outputs are generated within the clock tree.

125 MHz → AD9523-1 → Clock + SYSREF

TI

TIDA-010128 + ADC12DJ5200RF

03

Public architecture: LMK61E2 reference source, LMK00304 fan-out, LMK04828 distribution / SYSREF and LMX2594 synthesizer form a cascaded clock path for a 10.4 / 20.8 GSPS RF-sampling ADC system.

Published clocking: the on-board and external-reference modes use a 260 MHz reference; LMX2594 generates the 5.2 GHz sampling clock while LMK04828 generates FPGA reference and SYSREF signals.

Indicative FCom selection: FCO-3L-PG may be evaluated as a fixed 260 MHz reference only where LMK61E2 programmability is not required and the complete noise budget is satisfied. The generated 5.2 GHz node is outside the scope of discrete FCom oscillator selection.

260 MHz → LMK / LMX → RF ADC

ADI

AD9081-FMCA-EBZ + FPGA Carrier

04

Public architecture: AD9081 mixed-signal front end, HMC7044 clock generation, SYSREF distribution and high-speed JESD204 links to an FPGA platform.

Published source: the evaluation board uses a 100 MHz on-board crystal oscillator; HMC7044 generates device, FPGA-auxiliary and SYSREF outputs. Direct external clocking is also supported.

Indicative FCom selection: FCO-6P-PJ may be evaluated for a confirmed CMOS 100 MHz input; FCO-2L-UJ may be considered only for a documented differential input. The production schematic and HMC7044 input configuration determine the applicable option.

100 MHz → HMC7044 → MxFE + FPGA

Platform interpretation: these public designs are provided as architecture examples and do not constitute approved-vendor-list status or drop-in replacement approval. Any FCom recommendation applies only to a documented discrete-source node and must be verified against the target schematic, receiver data sheet and complete clock-noise budget.

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High-Speed ADC / DAC + JESD204 Timing Architecture

Representative placement from precision reference through clock conditioning, converter sample clock, SYSREF and FPGA transport.

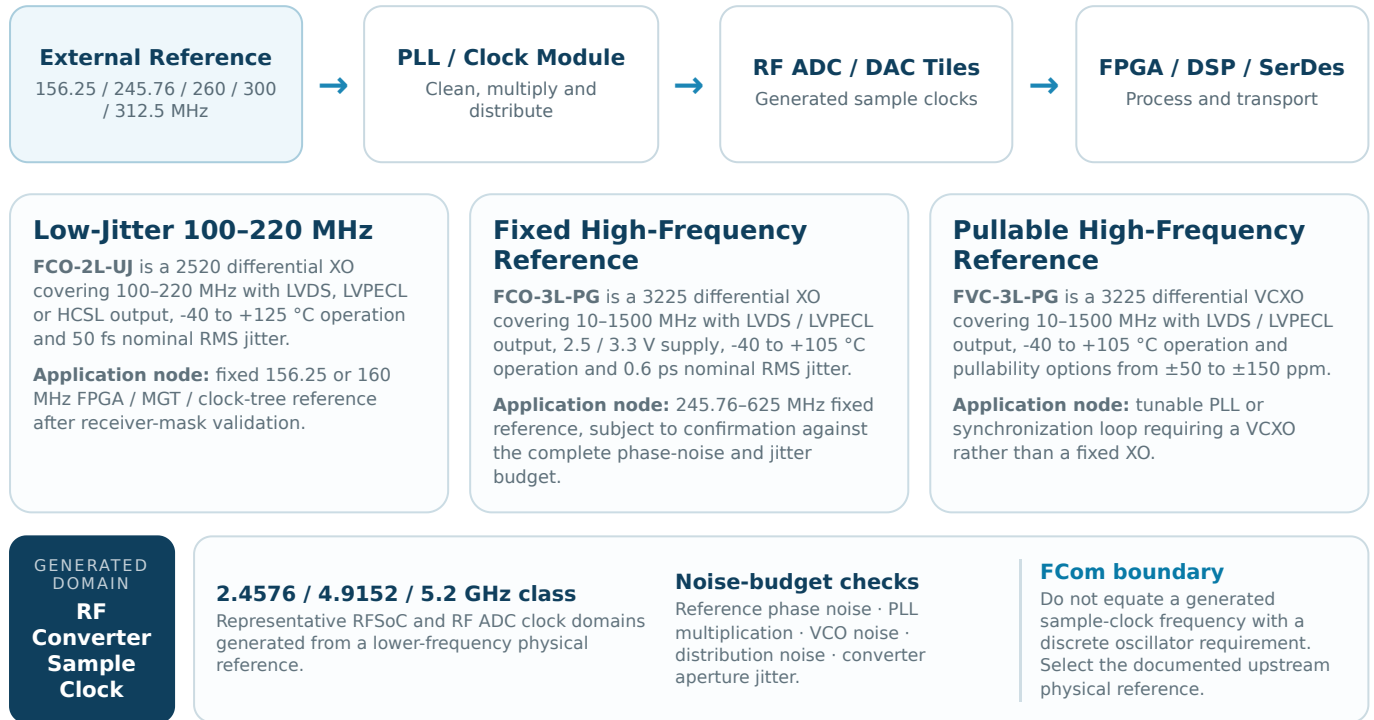


JESD204 note: device clock, FPGA reference and SYSREF are related but separate signals. Deterministic latency depends on their frequency plan, phase relationship and distribution path—not on a single oscillator specification.

06

RFSoc / FPGA + Direct-Sampling Timing Architecture

Representative reference planning for RFSoc tiles, high-speed data conversion, programmable processing and SerDes egress.



Architecture note: direct external sampling and PLL-multiplied sampling are different clock architectures. The preferred oscillator class, amplitude, phase-noise profile and frequency can change when the converter PLL is bypassed.

07

FCom Selection Guidance by Design Condition

This section presents FCom series with a clearly defined role in high-speed conversion and FPGA clock trees. Final frequency, output option and ordering code are confirmed by FCom engineering.

Precision 10 MHz

TCXO or low-noise OCXO master-reference path.

Compact CMOS

1–200 MHz programmable source into a confirmed CMOS input.

Low-jitter Differential

100–220 MHz fixed reference class with 50 fs nominal RMS jitter.

Up to 1.5 GHz

Fixed or pullable LVDS / LVPECL reference after system review.

Design Condition	FCom Selection	Current FCom Series Capability	Key Check Before RFQ
Compact high-stability master reference	FVT-7S-HP	7050 4-SMD TCXO; 5–52 MHz; 2.5 / 3.3 V; clipped sine or CMOS; ± 50 ppb; -40 to +105 °C; ± 5 ppm pullability.	10 MHz configuration · waveform · load · warm-up · aging
Low-noise precision master where the system accommodates power and warm-up requirements	FOC-5S-LN	14 × 9 mm 6-SMD OCXO; 10–40 MHz; 3.3 / 5 V; ± 5 ppb; -40 to +85 °C; listed phase-noise performance of -120 / -145 / -157 / -162 dBc/Hz at 10 Hz / 100 Hz / 1 kHz / 10 kHz.	Output compatibility · power · warm-up · aging · vibration
Compact programmable CMOS reference for a clock IC input	FCO-6P-PJ	2016 4-SMD; 1–200 MHz; 1.8 / 2.5 / 3.3 V; CMOS; ± 15 ppm; -40 to +125 °C; 0.8 ps nominal RMS jitter.	Programmed frequency · VDD · load · OE · jitter band
100–220 MHz low-jitter differential reference	FCO-2L-UJ	2520 6-SMD; 1.8 / 2.5 / 3.3 V; LVDS / LVPECL / HCSL; ± 20 ppm; -40 to +125 °C; 50 fs nominal RMS jitter.	Output variant · integration band · receiver mask · termination
245.76–625 MHz fixed or pullable differential reference	FCO-3L-PG / FVC-3L-PG	3225; 10–1500 MHz; 2.5 / 3.3 V; LVDS / LVPECL; -40 to +105 °C. FCO fixed-XO jitter is 0.6 ps; FVC pullability options are ± 50 to ± 150 ppm.	Fixed vs tunable · exact rate · phase-noise mask · loop design

Specification note: performance values shown are series-level reference values and must be evaluated using the applicable carrier frequency, integration band, test method and receiver mask. Final ordering code and guaranteed limits are confirmed in the product-specific FCom specification. Crystal filters, SAW resonators and SAW filters serve RF / IF functions and are outside the clock path shown here.

ENGINEERING SELECTION SUPPORT

Request an FCom Data-Conversion Timing Recommendation

Provide the converter, clock IC, FPGA / RFSoc or SerDes part number, physical clock pin, source topology, exact frequency, output logic, jitter / phase-noise requirement, tuning range, voltage, temperature, package and project stage.

[Request Engineering Review →](#)

08

Engineering Validation & Minimum RFQ

High-speed data-conversion timing must be validated against the complete clock path; frequency alone is not sufficient.

Converter / Clock IC

- Exact ADC / DAC and clock-IC part numbers
- Physical clock input and selected mode
- Direct clock or PLL-multiplied architecture
- Input amplitude and common-mode requirement
- Aperture-jitter / SNR target
- Supply-noise and thermal environment

JESD204 / SYSREF

- JESD204B or JESD204C subclass
- Device-clock frequency and SYSREF mode
- Deterministic-latency requirement
- One-shot, periodic or gated SYSREF
- Required skew / phase alignment
- FPGA transport and lane configuration

FPGA / RFSoc / SerDes

- Exact device and transceiver bank
- REFCLK pin and exact frequency
- LVDS / LVPECL / HCSL interface
- Receiver phase-noise or jitter mask
- Termination, swing and coupling
- Line rate, encoding and PLL mode

Master Reference / Environment

- XO, VCXO, TCXO, OCXO or external source
- Stability, aging and holdover target
- Pull range and control voltage
- RMS-jitter integration band
- Temperature, airflow and vibration
- Startup, warm-up, power and lifecycle

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	RF-sampling receiver, ADC / DAC board, RFSoc, FPGA / DSP, JESD204 link, digitizer, AWG or test instrument.
Target Device	Exact receiver and clock-IC part numbers, plus the physical clock pin or schematic location.
Clock Topology	Fixed XO, pullable VCXO, TCXO, OCXO, external reference, jitter cleaner, direct clock or PLL-multiplied path.
Electrical Requirements	Exact frequency, VDD, CMOS / LVDS / LVPECL / HCSL / sine, load, swing, termination, OE and startup state.
Performance Requirements	Stability, aging, phase-noise points or mask, RMS integration band, pull range, aperture-jitter budget and SYSREF behavior.
Program Requirements	Prototype quantity, sample date, validation plan, annual volume, production location, lifecycle and compliance documentation.

Same Frequency, Different Source

125 MHz may be a CMOS board XO, differential reference, pullable VCXO or generated clock-IC output.

Same Jitter, Different Band

Two RMS values are comparable only when carrier frequency, integration limits and measurement method match.

Same Platform, Different Mode

Direct clocking, internal PLL and external jitter-cleaner modes can require different source noise profiles.

Frequency alone does not define the final part: a complete recommendation requires the source architecture, receiver interface, phase-noise / jitter method, tuning requirement and system operating conditions.

09

Engineering FAQ & Application Review

Common data-conversion timing questions, public platform references and the information required for FCom engineering review.

Is the ADC or DAC sample rate the required oscillator frequency?

Not necessarily. A lower-frequency reference often feeds a PLL or clock generator that produces the multi-gigahertz sample clock.

Can the lowest published RMS-jitter number be selected directly?

No. The integration band, carrier frequency, phase-noise profile and complete PLL transfer function must match the receiver and SNR budget.

When is a VCXO preferred over a fixed XO?

A VCXO is used when a PLL, synchronization loop or frequency-control architecture requires pullability. A fixed XO does not provide that control range.

When are TCXO and OCXO products relevant?

They are appropriate at precision master-reference nodes where absolute stability, close-in noise, aging or holdover matters, provided the system also accommodates their power and warm-up requirements.

Are 122.88, 125 and 156.25 MHz interchangeable?

No. They belong to different platform plans and must match the exact receiving device, PLL configuration and interface.

Does JESD204 require only one clock?

No. Device clock, FPGA reference and SYSREF have distinct functions; deterministic latency depends on their relationship and distribution.

Can a generated 500 MHz output be replaced with a 500 MHz XO?

Only after redesigning and validating the clock tree. A generated output does not imply a standalone oscillator position.

Does a public evaluation platform confirm an approved FCom replacement?

No. It provides architectural context and identifies potential physical source nodes. Final selection requires review of the production schematic, receiver requirements and validation plan.

Representative Public Technical References

1. **AMD:** ZCU111 RFSoc evaluation platform.
2. **AMD:** ZCU111 clock generation and board reference domains.
3. **AMD:** ZCU111 RF data-converter clocking.
4. **Analog Devices:** AD-FMCDQA2-EBZ JESD204 system architecture.
5. **Analog Devices:** DAQ2 clocking and generated device / FPGA clocks.
6. **Texas Instruments:** TIDA-010128 RF-sampling clocking reference design.
7. **Texas Instruments:** ADC12DJ5200RF evaluation-module user guide.
8. **Analog Devices:** AD9081-FMCA-EBZ evaluation platform.
9. **Analog Devices:** AD9081 / AD9082 evaluation-board user guide and clock architecture.

FCom product specification note: product information in this guide is presented at series or representative-configuration level using FCom product information available at the time of publication. Exact ordering codes, guaranteed limits, frequency availability and receiver compliance must be confirmed in the applicable FCom specification and formal quotation.

ENGINEERING REVIEW

High-Speed Data Conversion Timing Review

Provide the exact converter, clock IC, FPGA, RFSoc or SerDes receiver; identify the physical clock pin, topology, frequency, supply, output logic, tuning range, phase-noise or jitter target, temperature range, package and project stage. FCom engineering can review the requirement and recommend an appropriate timing series and configuration for board-level validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection must be confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.