

VEHICLE COMPUTE & CONTROL

ECUs & Domain Controllers

Coordinate processor, network and retained-time references across automotive ECUs and domain controllers, with timing options suited to wide operating-temperature requirements.

Processor Timing + Network Clocking + Retained Time + Safety Domains + Wide Temperature

Body / Chassis ECUs

Gateway ECUs

Zonal Controllers

Domain Controllers

Vehicle Compute

Automotive Ethernet

Application Scope

Automotive control and compute platforms combining MCU / SoC processing, safety functions, CAN / CAN FD / LIN, Ethernet, high-speed interfaces and retained-time domains.

Selection Philosophy

Select by clock domain first. External crystals and oscillators are normally selected at documented MCU, SoC, PHY, FPGA or RTC reference inputs; internal CPU, CAN bit rate and SerDes line rate are derived system quantities.

Processor

Main MCU, safety MCU, SoC and FPGA reference timing.

Network

Automotive Ethernet PHY, switch, gateway and RMII reference clocks.

Retained Time

RTC, sleep / wake scheduling, event logging and low-power supervisory timing.

High-Speed

PCIe, SerDes, Ethernet and FPGA references in advanced domain-controller architectures.

01

Application Scope & Engineering Domains

Separate processor, network, retained-time, safety and high-speed reference domains before selecting a timing device.

ECUs & Domain Controllers spans architectures from a single automotive MCU through gateway and zonal controllers to high-performance SoC-based compute platforms. As functions consolidate, the timing problem shifts from one local controller reference toward coordinated processor, network, safety and high-speed interface clocks.

Typical Equipment

Conventional ECUs
Body Control Module
Chassis / Safety ECU
Powertrain ECU
Comfort / Actuation ECU

Gateway & Zonal
Central Gateway
Telematics / Service Gateway
Zonal Controller
Automotive Ethernet Switch Node

Domain & Vehicle Compute
ADAS Domain Controller
Cockpit / Fusion Controller
Vehicle Compute Platform
High-Performance Central Computer

Five Engineering Domains

Processor Timing
MCU / SoC / FPGA external reference and internal PLL-derived processing clocks.

Network Timing
Ethernet PHY / switch references plus controller-derived CAN / LIN timing.

Retained-Time
32.768 kHz RTC, sleep / wake and event timestamping where an external low-speed node exists.

Safety & Independence
Main / safety controller references, clock monitoring and independent safety domains.

Startup Margin
CL · ESR · drive level · negative resistance · startup across temperature.

Accuracy
Tolerance · temperature stability · aging · interface ppm budget.

Clock Interface
XTAL vs CLKIN · CMOS / LVDS / LVPECL / HCSL · OE / standby.

Environment
AEC qualification · local PCB temperature · vibration / thermal cycling · EMC.

Architecture boundary: CPU operating frequency, CAN / CAN FD bit rate, Ethernet line rate and PCIe / SerDes lane rate are typically generated within the device clock architecture. External crystal or oscillator selection should therefore follow the documented reference-clock input of the selected IC.

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Select by System Node First

Begin with the documented external clock node, then determine clock topology, frequency, performance class and qualification requirements.

The same ECU or domain controller can contain several timing domains. A reliable selection process begins with the receiving IC and its documented clock input, followed by the required frequency, interface and environmental conditions.

System Node	Typical Function	Representative External Reference	Typical Device	Selection Focus
Main MCU	Primary ECU processing reference	8 / 12 / 16 / 20 / 24 / 40 MHz class	MHz crystal / CMOS XO	XTAL vs CLKIN, CL / ESR, startup margin, AEC requirement
Safety MCU	Independent monitoring / fallback domain	16 / 20 / 24 / 40 MHz class	Crystal / CMOS XO	Clock independence, startup, qualification, thermal zone
Application SoC / Processor	Domain-controller compute reference	19.2 / 20 / 24 / 25 / 40 MHz class	Crystal / CMOS XO	Platform clock tree, PLL input, driven vs resonator input
Automotive Ethernet PHY	PHY reference	25 MHz	Crystal / CMOS XO	PHY oscillator mode, ppm budget, CL / output compatibility
RMII / Driven Network Clock	Externally supplied interface reference	50 MHz	CMOS XO	REF_CLK direction, logic level, duty cycle and loading
FPGA / PCIe / SerDes / High-Speed Ethernet	High-speed interface reference	100 / 125 / 156.25 MHz	Low-jitter CMOS / differential XO	RMS jitter, output logic, termination, signal integrity
RTC / Retained-Time	Sleep / wake / timestamp time base	32.768 kHz	Tuning-fork crystal / kHz XO	External RTC topology, CL, ESR, standby current

1 · Confirm the Clock Input

Identify XTAL pins, CLKIN / REF_CLK, differential REFCLK or low-speed RTC oscillator input from the target-device documentation.

2 · Classify the Requirement

Separate standard controller timing from retained-time, driven network clocking and high-speed low-jitter reference requirements.

3 · Apply Environment & Qualification

Confirm operating temperature, automotive qualification, package constraints and system-level startup / jitter margin before selecting a product series.

Recommended sequence: System node → external vs derived → crystal vs driven clock → frequency → electrical performance → qualification / temperature → package → FCom series → final configuration.

03

Frequency & Component Placement Matrix

Evaluate each frequency together with system position and clock topology. Internal processing, network line rates and peripheral clocks remain separate from the external reference.

System Position	Representative Frequency	Primary Function	Applicability	Preferred Device
RTC / Retained-Time	32.768 kHz	Sleep / wake / event timestamp	Common External Reference	Crystal / low-power kHz XO
Low-Frequency MCU	8 / 12 MHz	Automotive MCU reference	Platform-Dependent	MHz crystal
Main / Safety MCU	16 / 20 / 24 / 40 MHz	Controller reference	Common External Reference	Crystal / CMOS XO
Application SoC	19.2 / 20 / 24 / 25 / 40 MHz class	Processor / PLL reference	Platform-Dependent	Crystal / CMOS XO
Automotive Ethernet PHY	25 MHz	PHY oscillator reference	Common External Reference	Crystal / XO
RMII / Driven Network	50 MHz	Externally driven REF_CLK	Interface-Dependent	CMOS XO
Gateway / FPGA / PCIe / SerDes	100 / 125 / 156.25 MHz	High-speed interface REFCLK	Advanced Domain Controller	Low-jitter CMOS / differential XO
CPU / Internal PLL Domains	100 MHz to GHz class	Processing clocks	Often Internally Derived	Confirm whether an external reference is required
CAN / CAN FD / LIN	Protocol-dependent bit rate	Vehicle-network timing	Controller-Derived	Validate MCU reference and clock tree

Crystal-Input Nodes

Selection is primarily determined by frequency, CL, ESR, drive level, startup margin, temperature and automotive qualification.

Driven-Clock Nodes

Confirm supply, CMOS / differential logic, duty cycle, output loading, OE behavior and receiver clock specifications.

High-Speed REFCLK

For interfaces with dedicated high-speed reference inputs, include RMS jitter, integration bandwidth, termination and signal-integrity requirements in the selection criteria.

Network note: 25 MHz is a common Automotive Ethernet PHY reference, while 50 MHz is used by selected externally driven interfaces such as RMII. The exact PHY / MAC clock mode governs crystal versus oscillator selection.

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Representative Platform & Architecture Matrix

Four public platforms illustrate the progression from MCU-centric networked ECUs to zonal, gateway and high-performance domain-controller architectures. These examples are used to clarify clock-domain structure and selection priorities.

NXP

1

S32K3-T-BOX · Networked ECU / Telematics Gateway

Architecture: S32K344 MCU + SJA1110 automotive Ethernet switch with seven Ethernet, six CAN / CAN FD and four LIN interfaces. NXP also documents two clock generators for precise AVB references.

Clock evidence: S32K3 clock architecture supports an external fast reference in the 8–40 MHz class and a 32.768 kHz slow reference, while higher CPU / peripheral / FlexCAN clocks are internally derived.

Main MCU Ref.

→

S32K344 Clock Tree

→

CAN / LIN / Ethernet

Selection insight: MCU, retained-time and Ethernet / AVB reference domains represent separate clock-selection decisions within the same platform.

INFINEON + FLEX

2

Flex Zone Control Reference Kit · Zonal Controller

Architecture: dual AURIX TC4D9 MCUs with six Ethernet channels, 20 CAN-FD, 16 LIN, TSN routing, power distribution and local actuation.

Clock evidence: AURIX TC4x supports external crystal / SYSCLK inputs and independent System / Peripheral PLL domains. Public high-speed examples identify 20 / 25 / 40 / 50 MHz crystal / SYSCLK input classes.

Controller Ref.

→

Dual TC4D9

→

TSN / CAN / LIN / HSSL

Selection insight: one zonal controller can contain multiple controller and network clock domains with safety-monitoring requirements.

RENESAS

3

R-Car S4 Automotive Communication Gateway

Architecture: integrated MCU + application-SoC domains with 16 CAN FD, FlexRay, PCIe Gen4 and 5G-USXGMII Ethernet on one gateway platform.

Clock evidence: the public reference platform includes a flexible clock generator capable of 12 outputs, including automotive PCIe Gen1–4 and UFS clocking.

SoC / MCU Ref.

→

R-Car S4 + Clock Gen.

→

PCIe / Ethernet / Storage

Selection insight: central gateways shift from a single local crystal toward coordinated processor and multi-interface reference clocks.

TEXAS INSTRUMENTS

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TIDEP-01020 · High-Performance Domain Controller

Architecture: DRA829V / TDA4VM Jacinto 7 SoC platform with Ethernet, PCIe, CAN-FD, camera, display, GNSS / wireless connectivity and an integrated Safety MCU.

Clock evidence: TI J721E PLL documentation publishes input-crystal configurations including 19.2 MHz, 20 MHz and 24 MHz, with GHz-class processor and peripheral clocks generated internally by PLLs.

Processor Ref.

→

Jacinto 7 PLLs

→

SoC / Safety / Network / PCIe

Selection insight: advanced domain controllers require separate analysis of processor, safety and high-speed-interface references.

Platform interpretation: these public examples are provided to illustrate representative clock architectures. They do not imply FCom adoption, qualification, compatibility or drop-in replacement. Final component selection should be verified against the selected IC documentation, schematic and complete system requirements.

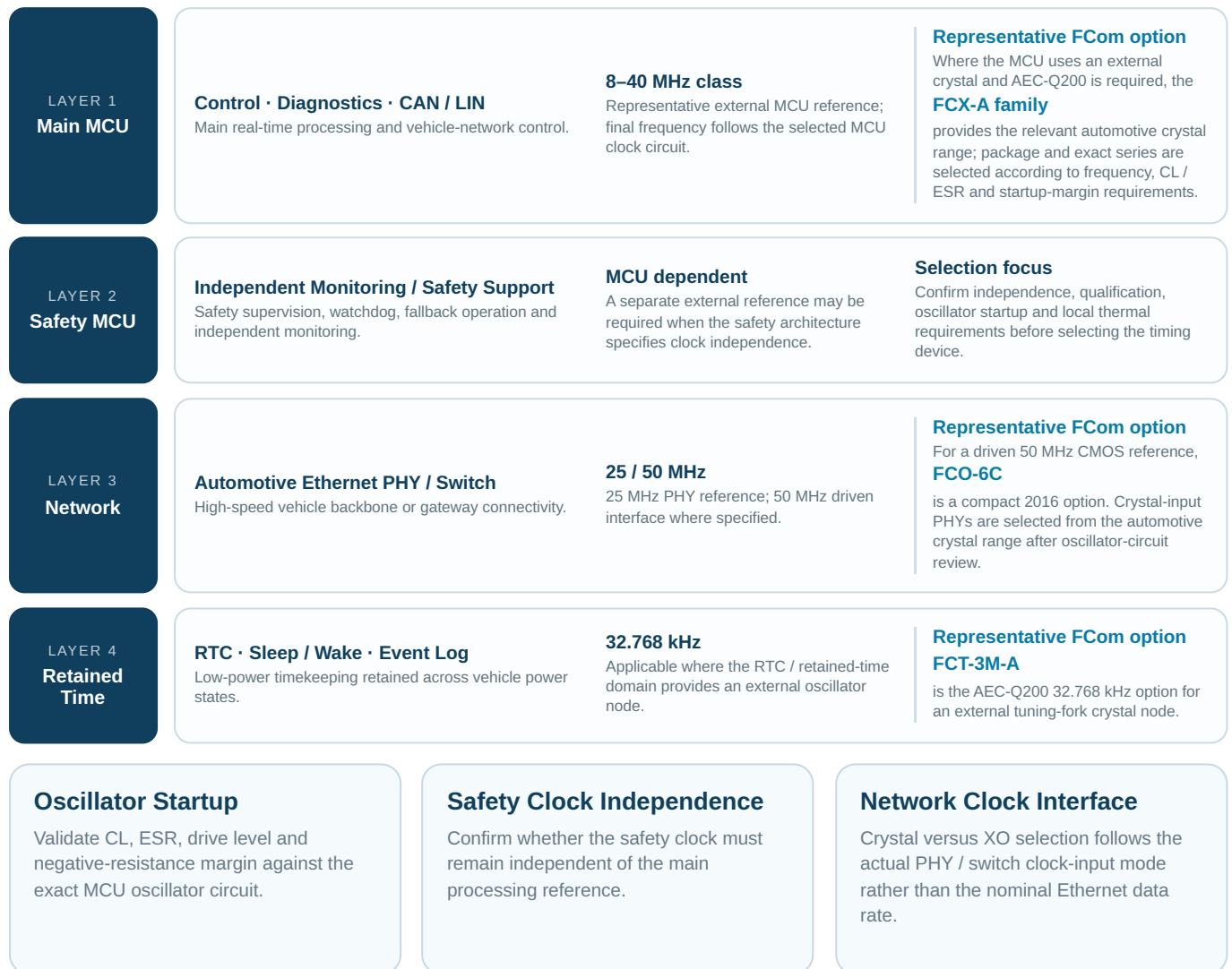
04 · Platform Evidence
Fuji Crystal (Hong Kong) Electronics Co., Ltd. · www.fujicrystal.com · General Inquiry: FCom@fujicrystal.com · Technical Support: support@fujicrystal.com

05

05

Conventional ECU / Gateway Timing Architecture

Representative placement of external timing in an MCU-centric ECU with safety, Automotive Ethernet and retained-time domains.

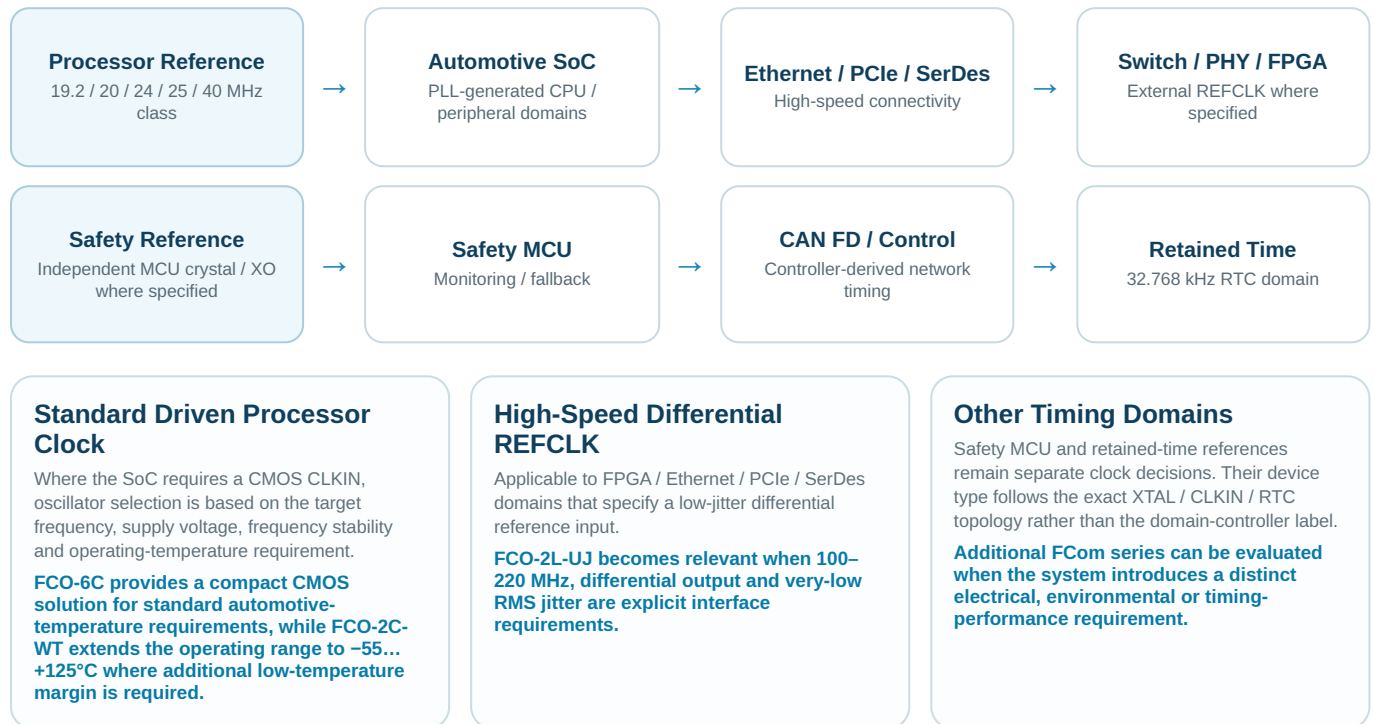


06

High-Performance Domain Controller Timing Architecture

Representative timing domains in a SoC-based vehicle-compute platform combining processor, safety, network and high-speed interface references.

System Clock Path



Architecture rule: a high-performance domain controller may contain several independent timing domains. Each documented clock input should be evaluated according to its own frequency, interface and jitter requirements rather than treating the controller as a single-frequency system.

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FCom Selection Guidance by Design Condition

The product families below correspond to the primary timing decisions encountered in ECU and domain-controller designs. Exact frequency, package and ordering code are confirmed after the target clock interface and electrical requirements are defined.

Automotive Crystal

MCU / safety-controller crystal input with an AEC-Q200 requirement.

Retained-Time

External 32.768 kHz tuning-fork crystal for automotive RTC / standby nodes.

Driven CMOS

Standard or wider-temperature CLKIN / REF_CLK path.

High-Speed Differential

Low-jitter differential REFCLK for advanced domain-controller interfaces.

Design Condition	FCom Selection	Why It Changes the Decision	Key Check Before RFQ
XTAL input + AEC-Q200	FCX-A family	The automotive crystal family is applicable when the receiving MCU / PHY provides an external resonator input and AEC-Q200 qualification is required. Package and exact FCX-A series are selected according to frequency, CL / ESR and oscillator-margin requirements.	Frequency · CL · ESR · startup margin · package
External automotive 32.768 kHz	FCT-3M-A	AEC-Q200 tuning-fork crystal for RTC / retained-time nodes that provide an external 32.768 kHz resonator input.	RTC topology · CL · ESR · standby requirement
Driven CMOS CLKIN / REF_CLK	FCO-6C FCO-2C-WT	FCO-6C provides a compact CMOS clock solution, while FCO-2C-WT is suited to designs requiring an operating range down to -55°C.	Frequency · VDD · ppm · temperature · OE / load
100–220 MHz + differential + explicit low jitter	FCO-2L-UJ	Applicable when the receiving FPGA / Ethernet / PCIe / SerDes interface specifies a differential low-jitter reference input.	LVDS / LVPECL / HCSL · jitter band · termination · VDD

Application-specific extensions: TCXO, VCXO, OCXO, programmable XO, spread-spectrum XO and RF/filter products are available for designs with specific accuracy, tuning, synchronization, EMI-management or filtering requirements. These device classes are evaluated when the system architecture introduces the corresponding function.

ENGINEERING SELECTION SUPPORT

Request an FCom Timing Recommendation

Provide the target MCU / SoC / PHY / FPGA, relevant clock input, frequency, CL / ESR or supply / output requirements, stability / jitter targets, operating temperature, qualification requirements and package constraints.

[Start Engineering Review →](#)

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Engineering Validation & Selection Checklist

Confirm the clock topology, electrical limits, safety requirements and operating environment before final component selection.

Quartz Crystal

- Frequency, CL, ESR, C0 and drive level
- Initial tolerance and temperature stability
- Negative resistance and startup margin
- Target MCU / PHY oscillator circuit
- AEC-Q200 / PPAP requirement where applicable

CMOS / Differential XO

- Supply voltage and input logic
- Duty cycle, rise / fall and OE behavior
- Termination / fan-out / signal integrity
- Jitter integration bandwidth where specified
- Local PCB temperature and qualification requirement

Retained-Time / RTC

- External crystal oscillator vs driven 32.768 kHz input
- CL / ESR or output-voltage requirement
- Standby-current budget
- Accuracy over temperature
- Confirm whether RTC / PMIC already integrates its timing element

Safety / Clock Independence

- Is the safety reference independent from the main processor clock?
- Clock-monitoring and fallback behavior
- Startup sequence and reset dependencies
- Shared vs separate PLL / reference domains
- Functional-safety requirement and diagnostic coverage

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Body / chassis ECU, gateway, zonal controller, domain controller or vehicle compute; identify main MCU, safety MCU, SoC, PHY, switch, FPGA or RTC node.
Target IC	Exact MCU / SoC / PHY / switch / FPGA part number and the relevant XTAL / CLKIN / RTC / REF_CLK pin or schematic section.
Quartz Crystal	Frequency, package, CL, ESR, C0 if available, tolerance, temperature stability, drive level and automotive qualification requirement.
XO / Differential XO	Frequency, supply, output logic, stability, temperature, jitter target, duty cycle, OE / standby and termination / load information.
Safety Architecture	Required clock independence, shared-clock dependencies, watchdog / monitoring concept and functional-safety requirements.
Project / Program	Prototype quantity, sample date, qualification timing, annual volume, SOP schedule, production site and reliability / environmental constraints.

Clock Architecture

Confirm XTAL vs CLKIN and external vs internally derived before comparing FCom families.

Thermal Zone

Specify the expected local PCB temperature at the timing device in addition to the vehicle ambient range.

High-Speed Reference

For 100 / 125 / 156.25 MHz, specify output logic, jitter band, termination and receiving interface.

Frequency alone does not define the final component: “25 MHz” may describe a crystal-input PHY or a driven processor reference; “156.25 MHz” still requires output logic, jitter, supply and termination. The final FCom ordering code is confirmed after the complete electrical specification has been defined.

09

Engineering FAQ & Application Review

Common interpretation questions, selection boundaries and representative public architecture references.

Does the CPU frequency equal the crystal frequency?

No. The external reference is typically multiplied or divided by internal PLLs and clock trees. Selection should be based on the documented oscillator or CLKIN requirement rather than the final CPU operating frequency.

Does CAN FD require a dedicated crystal?

Usually not. CAN / CAN FD timing is normally derived from the MCU clock tree. The external timing component is selected at the controller reference node.

Is 50 MHz always required for Automotive Ethernet?

No. Many PHYs use a 25 MHz crystal or reference, while selected RMII or driven-clock architectures use 50 MHz. Confirm the required clock mode from the selected PHY / MAC documentation.

Does every ECU need a 32.768 kHz crystal?

No. An external 32.768 kHz device is used where the retained-time, RTC or sleep / wake architecture provides a documented low-speed oscillator or clock input.

When is a differential XO necessary?

A differential XO is typically used for high-speed FPGA / Ethernet / PCIe / SerDes reference nodes that specify low-jitter differential inputs. Standard MCU reference clocks are normally addressed with crystal or CMOS XO solutions.

Does -40 to +125°C automatically mean AEC qualified?

No. Operating-temperature range and automotive qualification are separate attributes. AEC-Q200 qualification is confirmed from the applicable FCom product specification for the selected series and configuration.

Representative Public Technical References

1. **NXP**: S32K3-T-BOX — S32K344 networked ECU / telematics / gateway reference platform.
2. **Infineon**: Flex Zone Control Reference Kit — dual AURIX TC4D9 zonal-controller platform.
3. **Renesas**: R-Car S4 Automotive Communication Gateway Platform — integrated MCU / SoC gateway architecture with 12-output clock generator.
4. **Texas Instruments**: TIDEP-01020 — Jacinto 7 automotive domain-controller reference design.

FCom product specification note: product information in this guide is presented at the series or representative-configuration level. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

ECUs & Domain Controllers Timing Review

Provide the system position, target MCU / SoC / PHY / FPGA, clock node, required external frequency, CL / ESR or supply / output, stability / jitter targets, operating temperature, package constraints, qualification requirements and project stage. FCom can review the requirement and recommend an appropriate product series and configuration.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.