

DIGITAL COCKPIT & VEHICLE CONNECTIVITY

Digital Cockpit & Vehicle Connectivity

Coordinate processor, display, audio, Ethernet, GNSS and wireless clock domains across digital cockpit and connected-vehicle platforms.

Processor Timing + Display & Video + Audio Clocking + Ethernet / PCIe + GNSS & Wireless

Digital Instrument Cluster

Center Information Display

Premium Audio

Telematics / TCU

GNSS / V2X

Automotive Ethernet

Application Scope

Cockpit SoCs, display processors, HUD / video bridges, audio codecs and DSPs, Ethernet / PCIe interfaces, telematics processors, GNSS receivers and wireless connectivity modules.

Selection Philosophy

Select by receiving clock node first. Processor, audio, RF and high-speed interface clocks are separate timing domains even when they coexist on the same cockpit or connectivity platform.

Processor

SoC / GPU / MCU PLL references and controller clocks.

Display & Audio

HUD / video reference plus dedicated audio-family master clocks.

GNSS & Wireless

Precision RF / baseband timing for navigation, TCU and V2X.

High-Speed I/O

Ethernet, PCIe and SerDes clocks with explicit jitter / output requirements.

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Application Scope & Engineering Domains

Modern cockpit and connectivity platforms combine several clock classes with different accuracy, jitter, interface and qualification requirements.

One platform, multiple timing domains. A cockpit SoC, display bridge, audio codec, GNSS receiver and Ethernet / PCIe interface can each require a different external reference. Timing selection therefore begins with the receiving IC specification and its documented clock input, rather than with CPU speed, display pixel rate, audio sample rate or RF carrier frequency.

Typical Equipment

Digital Cockpit

Infotainment Head Unit
Digital Instrument Cluster
Center / Passenger Display
HUD / AR-HUD
Rear-Seat Entertainment

Audio & Multimedia

Audio Codec / DSP
DAC / ADC
Premium / Zonal Audio
ANC / Voice Processing
Radio / Multimedia Processing

Vehicle Connectivity

Telematics Control Unit
GNSS / Navigation
Wi-Fi / Bluetooth
Cellular / C-V2X
Automotive Ethernet / Gateway

Six Engineering Domains

Processor & Graphics

SoC / MCU external reference and PLL input.

Display & Video

Display processor, bridge and SerDes reference.

Audio Timing

Codec / DSP master clock and audio-family references.

Ethernet & High-Speed I/O

PHY, switch, PCIe and SerDes REFCLK.

GNSS & Navigation

Precision receiver / baseband reference.

Wireless Connectivity

Cellular, Wi-Fi / Bluetooth and V2X reference clocks.

Frequency Accuracy

Especially important for GNSS / wireless and precision timing paths.

RMS Jitter

Relevant to audio MCLK and explicit PCIe / Ethernet / SerDes REFCLK inputs.

Clock Interface

XTAL · CMOS CLKIN · clipped sine · LVDS / LVPECL / HCSL.

Environment

AEC qualification · operating temperature · startup · EMI / SI constraints.

Clock-definition note: CPU / GPU GHz frequency, display pixel clock, MIPI / eDP / HDMI line rate, 44.1 / 48 kHz audio sample rate, Wi-Fi / cellular / GNSS RF carrier and PCIe / Ethernet line rate belong to internal or interface timing domains and are distinct from the external reference clock.

02

Select by System Node First

Begin with the receiving IC and its clock input, then determine the required frequency, device class, precision level and environmental requirements.

System Node	Clock Role	Representative External Reference	Typical Device	Selection Focus
Cockpit SoC / MCU	Processor PLL / main reference	16 / 19.2 / 20 / 24 / 25 / 27 / 33.33 / 40 MHz class	Crystal / CMOS XO	XTAL vs CLKIN, startup, ppm, thermal zone
Display / HUD Processor	Video / display reference	27 MHz class other platform-dependent values	Crystal / CMOS XO	Reference input vs internal pixel / video PLL clocks
Audio Codec / DSP	Audio master clock	12.288 / 24.576 / 49.152 MHz	Crystal / low-jitter CMOS XO	Audio family, jitter, ppm, clock distribution
Automotive Ethernet	PHY / switch reference	25 / 50 MHz class	Crystal / CMOS XO	PHY mode, CL / ESR or driven-clock interface
GNSS / Telematics	RF / baseband precision reference	26 / 38.4 MHz class	TCXO / crystal / XO	temperature stability, phase noise, startup, VDD
Wi-Fi / Bluetooth	Connectivity chipset reference	24 / 32 / 37.4 / 48 MHz class	Crystal / XO	chipset-specific reference and sleep-clock architecture
PCIe / High-Speed SerDes	High-speed REFCLK	100 / 125 / 156.25 MHz	Low-jitter CMOS / differential XO	RMS jitter, output logic, termination, signal integrity
RTC / Retained Time	Sleep / event-time reference	32.768 kHz	Tuning-fork crystal / kHz XO	CL, ESR, standby current, qualification

1 · Identify the Clock Input

Identify whether the target device uses XTAL pins, CMOS CLKIN, a clipped-sine RF reference or a differential REFCLK.

2 · Classify the Timing Domain

Evaluate processor / display, audio-family, GNSS / wireless precision and high-speed interface requirements as distinct timing domains.

3 · Apply Environment & Qualification

Define the local operating temperature, AEC requirement, package and system-level startup / jitter / phase-noise limits.

Recommended sequence: System node → clock input type → frequency → performance class → temperature / qualification → package → FCom series → final electrical configuration.

03

Frequency & Component Placement Matrix

Use frequency together with clock-domain function and interface type. Similar frequencies can belong to very different system nodes.

Frequency / Family	Representative System Position	Applicability	Selection Interpretation
32.768 kHz	RTC / GNSS / wireless sub-clock	Secondary External Reference	Used where retained-time or low-power sub-clock is provided externally.
12.288 / 24.576 / 49.152 MHz	Audio codec / DSP / audio-video master clock	Common Audio Reference	48 kHz-family MCLK references; sample rate itself is not the oscillator frequency.
16 / 19.2 / 20 / 33.33 / 40 MHz	Cockpit MCU / SoC / telematics processor	Platform-Dependent	External processor reference selected from the SoC / MCU oscillator interface.
24 / 25 / 27 MHz	Processor / display / USB / SerDes / Ethernet	Common External Reference	High-usage standard references across cockpit and interface nodes.
26 / 38.4 MHz	GNSS / telematics / RF reference	Precision RF Reference	Often moves the selection toward TCXO when tighter stability / phase noise is required.
32 / 37.4 / 48 MHz	Wi-Fi / Bluetooth / USB connectivity	Wireless Platform Reference	Follow the exact wireless chipset requirement; RF carrier frequency is separate.
50 / 52 MHz	SerDes / Ethernet / processor / telematics	Interface-Dependent	50 MHz commonly serves driven interface clocks; 52 MHz can appear in telematics / RF timing.
100 / 125 / 156.25 MHz	PCIe / Ethernet / high-speed SerDes	High-Speed Extension	Low-jitter CMOS or differential reference; output logic and jitter become first-order criteria.

Audio-Family Extension

11.2896 / 22.5792 / 45.1584 MHz may appear in 44.1 kHz-family audio systems. They are treated as application-dependent until confirmed by the selected codec / DSP architecture.

Platform-Specific Audio / Video

18.432 / 55.46667 / 62.4 MHz appear in published automotive IVI mappings and are best treated as platform-specific references.

Display Interpretation

27 MHz is a common external video / HUD reference, while pixel clocks and display-link rates are normally generated inside the video chain.

Reference-clock interpretation: CPU / GPU clock, display pixel rate, audio sample rate, 5G / Wi-Fi / GNSS RF carrier, PCIe lane rate and Ethernet data rate are separate from the external reference used by the receiving IC.

04

Representative Platform & Architecture Matrix

Four public platforms illustrate central cockpit compute, head-unit multimedia, connected-vehicle networking and multi-output clock distribution. They are used as architecture evidence only.

QUALCOMM

1

Snapdragon Cockpit Platform · Central Cockpit Compute

Architecture: scalable cockpit compute supporting multiple high-resolution displays, premium / zonal audio, navigation, Wi-Fi / Bluetooth and virtualized processing.

Clock evidence: the public platform demonstrates coexistence of processor, graphics, display, audio and wireless domains; board-level reference frequencies remain platform-specific.

Processor / Graphics → Display & Audio → Wireless Services

Selection insight: processor, display, audio and wireless references form independent clock domains within the overall cockpit architecture.

TEXAS INSTRUMENTS

2

TIDEP-0097 · Head Unit Display Audio Reference Design

Architecture: Jacinto DRA71x-based infotainment / digital-cluster design supporting HDMI, USB 3.0 / 2.0, FPD-Link, TAS6424 digital Class-D audio and 100BASE-T1 Ethernet PHY devices.

Clock evidence: a single head unit combines processor, display / SerDes, audio, USB and Ethernet timing domains on the same PCB.

DRA71x SoC → Display / Audio / USB → Ethernet

Selection insight: timing is selected at the individual receiving IC, while video, audio and network data rates remain separate interface parameters.

NXP

3

OrangeBox 2.0 · Connectivity Domain Controller

Architecture: i.MX 94 platform integrating Wi-Fi 6E / Bluetooth 5.3, 5G cellular, DSRC V2X, precision GNSS, radio tuner and multi-gigabit Ethernet.

Clock evidence: wireless, GNSS, radio and Ethernet subsystems coexist under one connectivity controller but retain separate chipset-level reference requirements.

GNSS / Cellular → i.MX 94 Connectivity → Wi-Fi / BT / Ethernet

Selection insight: RF carrier frequency and external timing reference are separate parameters; each connectivity IC is evaluated from its documented reference input.

RENESAS

4

R-Car E3 Ebisu · Full Graphics Cluster & Clock Distribution

Architecture: R-Car E3 integrated-cockpit platform paired with a flexible 9FGV0841 clock generator.

Clock evidence: the clock generator can provide eight PCIe Gen1–4 clock outputs, allowing one device to replace several discrete crystal oscillators.

Reference Clock → Clock Generator → SoC / PCIe / Display

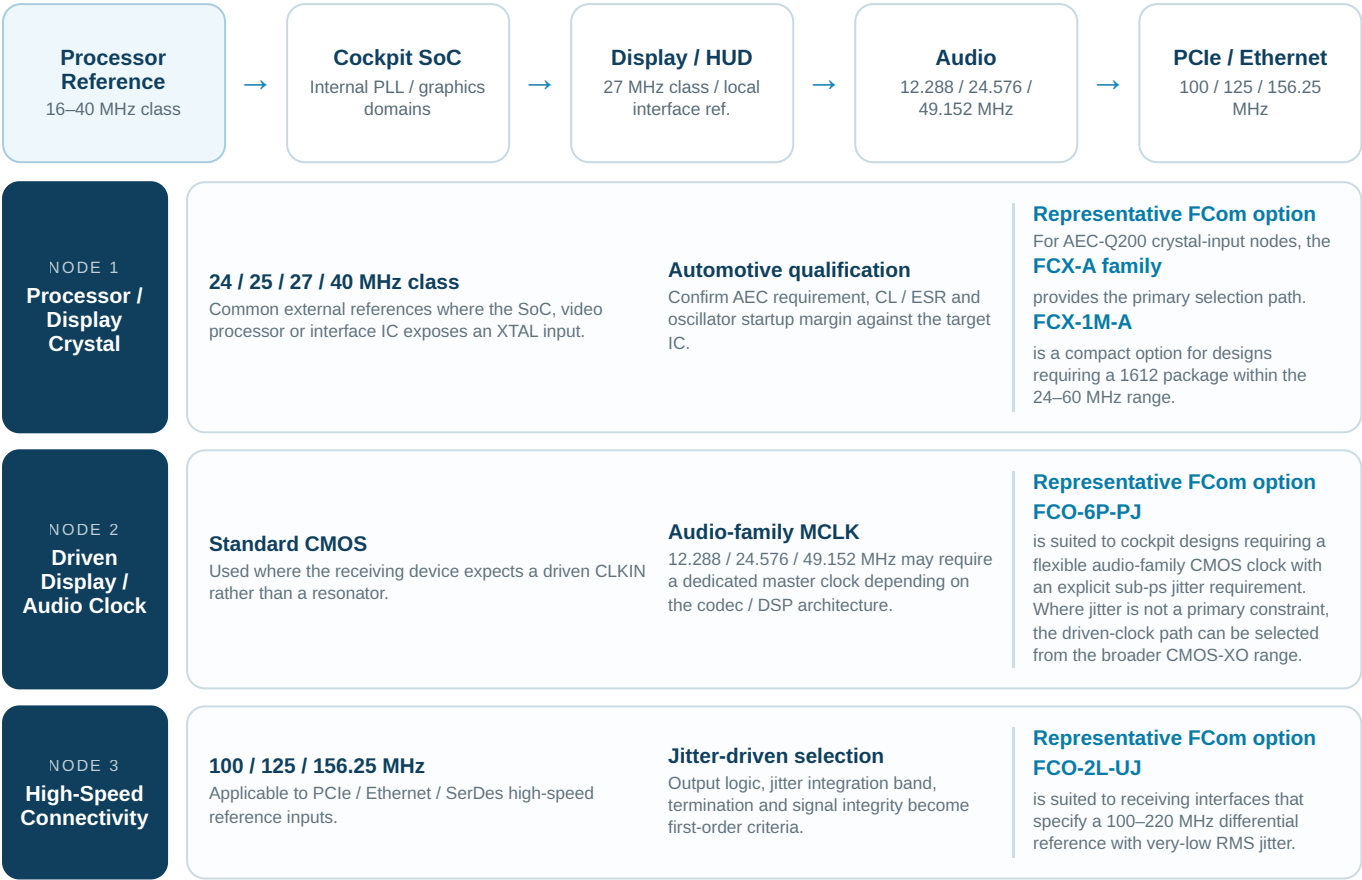
Selection insight: high-integration cockpit systems may consolidate several clocks through a coordinated clock-tree and distribution architecture.

Platform interpretation: these public examples are provided to illustrate representative timing architectures. They do not indicate FCom adoption, qualification, compatibility or drop-in replacement. Final component selection is based on the exact target-device documentation, schematic and complete system requirements.

05

Digital Cockpit & Multimedia Timing Architecture

Representative external timing from the cockpit processor into display, audio and high-speed interface domains.

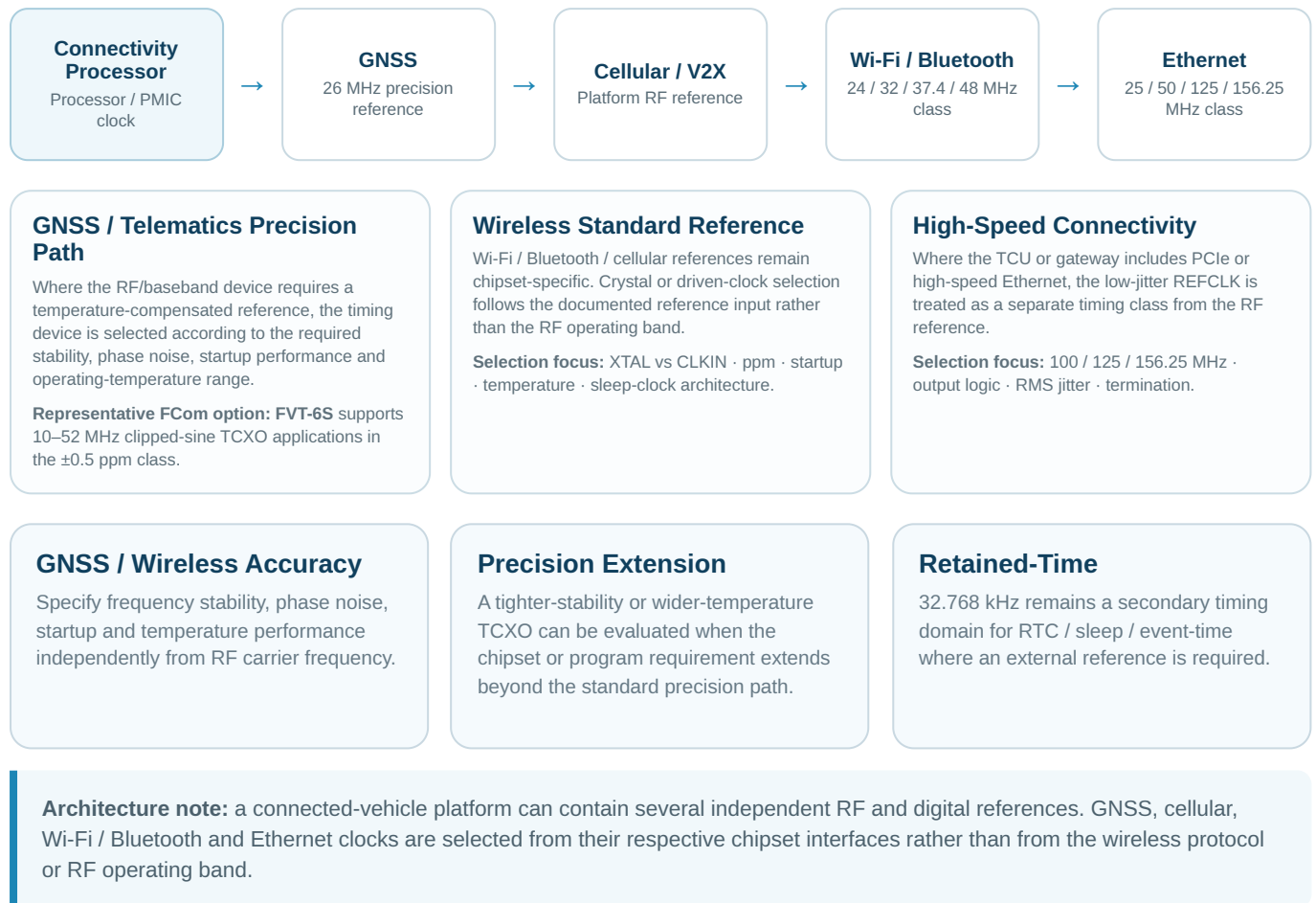


Architecture note: display pixel clocks and audio sample rates are separate from the external oscillator frequency. The timing device is selected from the processor / bridge / codec / DSP clock input and the clock-distribution architecture used across the multimedia system.

06

Connected Vehicle / Telematics Timing Architecture

Representative GNSS, cellular, Wi-Fi / Bluetooth and Ethernet timing around a vehicle connectivity processor.



07 FCom Selection Guidance by Design Condition

The product families below correspond to the primary timing decisions in digital cockpit and connected-vehicle architectures. Exact ordering codes are confirmed after the receiving clock interface is defined.

Automotive Crystal Input
 Processor / display / Ethernet XTAL input with AEC-Q200 requirement.

Audio / Driven Clock
 Dedicated audio-family or driven CMOS reference where jitter is an explicit requirement.

Precision GNSS / Wireless
 TCXO path for tighter ppm / phase-noise requirements.

High-Speed Differential REFCLK
 PCIe / Ethernet / SerDes low-jitter reference.

Design Condition	FCom Selection	Why It Changes the Decision	Key Check Before RFQ
XTAL input + AEC-Q200	FCX-A family	The automotive crystal family applies where the processor, display bridge, Ethernet or connectivity IC exposes an external resonator input and requires AEC-Q200.	Frequency · CL · ESR · startup margin · package
Audio-family / driven CMOS clock with explicit jitter requirement	FCO-6P-PJ	Applicable to 12.288 / 24.576 / 49.152 MHz-class audio or multimedia clocks that require a flexible driven source with tighter jitter than a standard CMOS reference.	Frequency · VDD · jitter band · output load · OE
26 / 38.4 MHz-class precision RF reference	FVT-6S	Applicable where GNSS / telematics / wireless timing requires tighter frequency stability and phase-noise performance than a standard crystal or XO path.	Frequency · VDD · stability · phase noise · temperature
100–220 MHz + differential + explicit low jitter	FCO-2L-UJ	Applicable to PCIe / Ethernet / SerDes interfaces that specify a differential low-jitter reference.	LVDS / LVPECL / HCSL · jitter band · termination · VDD
External automotive 32.768 kHz	FCT-3M-A	Dedicated AEC-Q200 tuning-fork crystal for RTC / sleep / event-time nodes that require an external 32.768 kHz resonator.	RTC topology · CL · ESR · standby requirement

Application-specific extensions: higher-precision / wider-temperature TCXO, VCXO / VCTCXO, OCXO, programmable XO, spread-spectrum XO and RF/filter products can be evaluated when the system introduces specific accuracy, tuning, holdover, EMI-management or filtering requirements. These device classes complement the core cockpit timing paths shown above where the corresponding function is required.

ENGINEERING SELECTION SUPPORT

Request an FCom Cockpit / Connectivity Timing Recommendation

Provide the target SoC / display / codec / GNSS / wireless / PHY device, clock input, frequency, CL / ESR or supply / output, jitter / phase-noise target, temperature, qualification and package constraints.

[Start Engineering Review →](#)

08

Engineering Validation & Minimum RFQ

Digital cockpit and connectivity timing is defined by the receiving node, clock topology and performance limits in addition to frequency.

Processor / Display

- SoC / MCU / display / bridge P/N
- XTAL or CLKIN requirement
- Frequency, CL / ESR or VDD / logic
- Startup / ppm requirement
- Local PCB temperature and AEC requirement

Audio

- Codec / DSP / DAC / ADC P/N
- MCLK frequency and audio family
- Local or SoC-generated master clock
- RMS jitter / phase-noise target if specified
- VDD / output / package

GNSS / Wireless

- GNSS / modem / Wi-Fi / BT / V2X chipset P/N
- Crystal / XO / TCXO input mode
- Reference frequency and ppm requirement
- Phase noise / startup if specified
- Temperature / tuning / supply

Ethernet / PCIe / SerDes

- PHY / switch / PCIe / SerDes P/N
- REFCLK frequency
- CMOS / LVDS / LVPECL / HCSL
- RMS jitter and integration band
- Termination / load / OE / supply

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	Cockpit SoC, display / HUD, audio codec / DSP, Ethernet / PCIe, GNSS, telematics, Wi-Fi / Bluetooth, V2X or RTC.
Target Device	Exact receiving IC part number and relevant clock pin or schematic location.
Clock Topology	External resonator, driven CMOS, clipped-sine precision reference, differential REFCLK or centrally distributed clock.
Crystal	Frequency, package, CL, ESR, tolerance, temperature stability, drive level and AEC-Q200 requirement where applicable.
XO / TCXO / Differential	Frequency, VDD, output logic, stability, temperature, RMS jitter / integration band, phase noise, tuning requirement, termination and OE.
Program	Prototype quantity, sample date, validation plan, annual volume, SOP timing, production site and qualification documentation.

Audio Family ≠ Sample Rate

The actual MCLK required by the codec / DSP should be identified in addition to the 44.1 kHz or 48 kHz audio sample rate.

RF Carrier ≠ Reference Clock

GNSS / Wi-Fi / cellular RF bands are separate from the crystal / TCXO reference frequency.

Temperature ≠ Qualification

Operating-temperature range and automotive qualification are separate attributes and are specified independently.

Frequency alone does not define the final component: a 25 MHz node may use an Ethernet crystal, a driven SerDes clock or a processor reference, while a 26 MHz node may require either a standard interface clock or a precision GNSS TCXO. The receiving IC and performance requirements determine the appropriate FCom solution.

09

Engineering FAQ & Application Review

Common digital-cockpit and vehicle-connectivity clock questions, representative public references and the information required for FCom engineering review.

Is CPU / GPU operating frequency the external oscillator frequency?

No. The external crystal or oscillator feeds a reference / PLL input; GHz-class processor clocks are normally synthesized internally.

Is display pixel clock the same as the crystal frequency?

Not necessarily. For example, automotive video processors can use a fixed external reference while generating much higher pixel / interface clocks internally.

Why are 12.288 / 24.576 / 49.152 MHz common in automotive audio?

They are widely used master-clock frequencies associated with 48 kHz-family audio processing. The codec / DSP clock architecture determines whether a dedicated crystal or XO is required.

Is 2.4 / 5 / 6 GHz Wi-Fi or a GNSS L-band frequency the crystal frequency?

No. Those values describe RF operating bands. The external reference is defined separately by the wireless or GNSS chipset.

When should a TCXO be considered?

A TCXO is appropriate when GNSS / telematics / wireless requirements call for tighter temperature stability, phase noise or frequency accuracy than a standard crystal / XO can provide.

When does a differential XO become necessary?

A differential XO is appropriate when PCIe, Ethernet or SerDes receivers explicitly specify a low-jitter differential REFCLK such as LVDS, LVPECL or HCSL.

Does every cockpit function need its own oscillator?

No. Integrated clock generators or distributed clocks can serve several interfaces when the architecture is designed for shared timing.

Does -40...+125°C automatically mean automotive qualified?

No. Operating-temperature range and AEC qualification are separate attributes. Qualification is confirmed from the applicable FCom product specification and the documentation required for the automotive program.

Representative Public Technical References

1. **Qualcomm:** Snapdragon Cockpit Platform — multi-display, premium audio, navigation and Wi-Fi / Bluetooth cockpit architecture.
2. **Texas Instruments:** TIDEP-0097 — DRA71x head-unit display-audio reference design with FPD-Link, USB, audio and 100BASE-T1 Ethernet components.
3. **NXP:** OrangeBox 2.0 — i.MX 94 connectivity domain controller with Wi-Fi 6E, Bluetooth 5.3, 5G, V2X, precision GNSS and multi-gigabit Ethernet.
4. **Renesas:** R-Car E3 Ebus — integrated-cockpit board using an 8-output PCIe Gen1–4 flexible clock generator.
5. **NDK:** Connected / Infotainment block diagram — public frequency mapping for MCU / SoC, audio/video, USB, GNSS, wireless, Ethernet and SerDes nodes.
6. **Renesas:** RAA278831 automotive HUD video processor — single 27 MHz crystal with internally generated video clocks.

FCom product specification note: product information in this guide is presented at series or representative-configuration level. Exact ordering codes, qualification status, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

Digital Cockpit & Vehicle Connectivity Timing Review

Provide the target SoC / display / codec / GNSS / modem / wireless / PHY part number, clock input, frequency, CL / ESR or supply / output, jitter / phase-noise targets, operating temperature, qualification and project stage. FCom can review the requirement and recommend an appropriate timing series and configuration.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.