

DIFFERENTIAL OUTPUT SERIES

Differential Output Crystal Oscillators

LVPECL, LVDS, and HCSL reference clocks for high-speed networking, PCIe, optical communication, and computing systems.

Standard Differential XO · Wide-Frequency PG XO · Voltage-Controlled References

PCIe & Computing

Ethernet & SmartNICs

Optical Transport

FPGA & SerDes

Clock Distribution

PLL & Synchronization

Portfolio Scope

FCom fixed-frequency XO and voltage-controlled VCXO families provide complementary LVPECL, LVDS, and HCSL clock outputs across compact 2520 through 7050 SMD packages.

Selection Approach

Begin with the receiver interface. Confirm the clock function, frequency, phase-jitter budget, supply rail, package, coupling, and termination before selecting a series.

3 Interfaces

LVPECL, LVDS, and HCSL differential output options

1.5 GHz

Highest listed frequency for designated PG XO and VCXO families

0.15 ps

Listed RMS phase-jitter reference for standard differential XO families*

2520–7050

Compact through larger SMD package options

*Listed integrated RMS phase jitter, 12 kHz to 20 MHz. Confirm carrier frequency, output, supply, load, temperature, and typ./max. classification for the selected configuration.

Standard Differential XO

Fixed Reference Clocking

Compact fixed-frequency solutions for LVPECL, LVDS, or HCSL receiver interfaces.

FCO-2L · FCO-3L · FCO-5L · FCO-7L

High-Frequency XO

Wide-Frequency Clocking

LVPECL and LVDS PG families extending differential fixed-reference coverage to 1.5 GHz.

FCO-3L-PG · FCO-5L-PG · FCO-7L-PG

Differential VCXO

Tunable Reference Clocking

Voltage-controlled references for PLL, frequency tracking, and synchronization functions.

FVC-3L-PG · FVC-5L-PG · FVC-7L-PG



01

Choose the Right Differential Architecture

Use the series-level data to develop a shortlist, then confirm the latest controlled datasheet for the exact orderable configuration.

Match the receiver before comparing packages. The selected output type must be compatible with the receiver input, common-mode range, coupling method, termination network, supply rail, and required timing performance.

Standard Differential XO						
				Fixed-frequency reference · listed jitter values: 12 kHz to 20 MHz		
Series	Package	Frequency	Output	Supply	Stability / Temp.	Jitter Ref.
FCO-2L / 3L / 5L / 7L	2520 / 3225 / 5032 / 7050 · 6-SMD	13.5–220 MHz: LVDS / LVPECL 100–135 MHz: HCSL	LVPECL, LVDS, HCSL	LVDS/HCSL: 1.8 / 2.5 / 3.3 V LVPECL: 2.5 / 3.3 V	±25 ppm -40 to +105°C	0.15 ps RMS

High-Frequency Differential XO				
			Fixed-frequency reference · LVPECL / LVDS	
Series / Family	Package	Frequency	Output & Supply	Timing Reference
FCO-3L-PG / 5L-PG / 7L-PG	3225 / 5032 / 7050 · 6-SMD	10–1500 MHz	LVPECL / LVDS 2.5 / 3.3 V	±25 ppm; -40 to +105°C; 0.6 ps RMS listed reference (12 kHz–20 MHz)

Differential VCXO				
			Voltage-controlled reference · LVPECL / LVDS	
Series / Family	Package	Frequency	Output & Supply	Tuning / Control
FVC-3L-PG	3225 · 6-SMD	10–1500 MHz	LVPECL / LVDS 2.5 / 3.3 V	Listed pullability options from ±50 to ±150 ppm
FVC-5L-PG / 7L-PG	5032 / 7050 · 6-SMD	10–1500 MHz	LVPECL / LVDS 2.5 / 3.3 V	±50 ppm APR listed; confirm the selected control range

Receiver Interface

Choose LVPECL, LVDS, or HCSL according to the receiving IC and the defined interface conditions.

Fixed or Tunable

Use an XO for a fixed reference or a VCXO when the system must control or track frequency.

Frequency Coverage

Use standard FCO-L families through 220 MHz or designated PG families through 1.5 GHz.

Timing Definition

State the phase-jitter integration band and any phase-noise or spur requirements.

Interface and timing qualification: An output label or frequency match does not establish compliance with PCIe, Ethernet, SerDes, or another interface standard. Confirm output swing, common-mode voltage, coupling, termination, receiver limits, timing masks, and the complete applicable test conditions.

02

Select by Receiver and Clock Role First

Identify the receiving interface and clock function before comparing oscillator packages or headline frequency ranges.



PCIe & Computing Reference Clocks

Role: Differential reference clock for PCIe-oriented or computing clock inputs.

Focus: HCSL receiver requirements, 100 MHz configuration, SSC, coupling, termination, and applicable timing mask.

FCO-2L / FCO-3L HCSL configurations as initial starting points

Ethernet Switches & SmartNICs

Role: PHY, switch, packet-processing, or data-path reference clock.

Focus: Receiver output type, 125 or 156.25 MHz frequency plan, RMS jitter band, rail, and temperature.

FCO-L LVDS or LVPECL configurations; PG families where required

Optical Modules & Transport

Role: SerDes, line-card, optical-interface, or recovered-clock reference.

Focus: Phase jitter, phase noise, output swing, common-mode range, coupling, and frequency-control requirements.

FCO-L / FCO-L-PG for fixed clocks · FVC-L-PG when tuning is required

FPGA, ASIC & SerDes

Role: High-speed transceiver, logic, or fabric reference clock.

Focus: Receiver-compatible interface, carrier frequency, jitter allocation, termination, and source placement.

FCO-L or FCO-L-PG according to frequency and interface requirements

Clock Distribution & Buffer Trees

Role: Low-noise source for a clock buffer or multi-device reference tree.

Focus: Source jitter, downstream additive jitter, fanout loading, pair routing, and regulator noise.

FCO-L family; review the complete source-to-receiver clock budget

PLL & Frequency Synchronization

Role: Electrically tunable reference for PLL, tracking, or synchronization functions.

Focus: Pullability, APR, control-voltage range, tuning gain, loop bandwidth, and phase noise.

FVC-3L-PG / FVC-5L-PG / FVC-7L-PG

Match the receiver

Confirm the input standard, common-mode range, coupling, differential load, and termination topology before selecting an oscillator output.

Define the timing target

State the carrier frequency, integration range, typ./max. limit, phase-noise offsets, output, supply, load, and temperature.

Validate the entire path

Review oscillator, power rail, termination, PCB routing, clock buffer, and receiving IC as one signal path.

Board-level guidance: Place the lowest-jitter source close to the consuming IC or clock buffer, maintain controlled differential impedance and a continuous return path, minimize stubs, isolate supply noise, and confirm the required termination location. Final suitability depends on system-level validation.

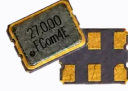
03

Shortlist by Interface and Clock Function

Each featured series represents an engineering starting point. The final orderable part number is determined by the complete electrical, timing, mechanical, and environmental requirements.

Compact Differential XO

FCO-2L



Compact fixed-frequency starting point for LVPECL, LVDS, or HCSL receiver interfaces.

2520 · 6-SMD

Compact package

13.5–220 MHz

LVDS / LVPECL range

100–135 MHz

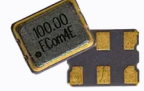
HCSL range

0.15 ps RMS

Listed ref. · 12 kHz–20 MHz*

Versatile Differential XO

FCO-3L



Balanced package option for networking, computing, and high-speed digital reference clocks.

3225 · 6-SMD

Package format

LVPECL / LVDS / HCSL

Output options

1.8 / 2.5 / 3.3 V

Supply options by output

±25 ppm

Listed stability

High-Frequency XO

FCO-5L-PG



5032 fixed-frequency PG-series starting point when the required frequency extends beyond the standard XO range.

5032 · 6-SMD

Package format

10–1500 MHz

Frequency range

LVPECL / LVDS

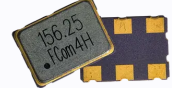
Output options

0.6 ps RMS

Listed ref. · 12 kHz–20 MHz*

Differential VCXO

FVC-7L-PG



7050 tunable differential starting point for PLL, frequency-tracking, and synchronization functions.

7050 · 6-SMD

Package format

10–1500 MHz

Frequency range

LVPECL / LVDS

Output options

±50 ppm APR

Listed control reference

Minimum RFQ Information

System node

Application, receiving IC, and applicable interface standard.

Clock function

Fixed XO or tunable VCXO, with the exact nominal frequency.

Electrical interface

LVPECL, LVDS, or HCSL; supply, coupling, load, and termination.

Timing requirements

RMS phase-jitter limit and integration band; phase-noise offsets if applicable.

Stability & environment

Frequency stability, operating temperature, package, and height.

Project requirements

SSC or enable requirements, annual usage, schedule, and documentation.

FCom Engineering Review Can Confirm

Output / Receiver Match

Compatible logic level, swing, common-mode range, and supply.

Coupling & Termination

Applicable load, network topology, and placement conditions.

Timing Conditions

Carrier, integration band, typ./max., phase-noise offsets, and test setup.

VCXO Control

Pullability, APR, control range, gain, and loop requirements.

Mechanical Configuration

Package, height, land pattern, and orderable options.

Verification Package

Controlled datasheet, test data, screening, and documentation as applicable.

TALK TO FCOM

Request a Differential Clock Review

Share the receiver interface, clock role, frequency, supply, jitter band, termination, stability, temperature, and package constraints. FCom can help identify suitable series and a practical board-level verification path.

* Series-level listed references. Confirm the exact orderable configuration, typ./max. status, integration band, and test conditions.

GENERAL INQUIRY

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TECHNICAL SUPPORT

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Product Information