

PRECISION TIME · HARDWARE TIMESTAMPING · AI FABRICS · HIGH-SPEED I/O

Data Centers & Cloud Timing

Enable precise timestamping, PTP synchronization and low-jitter clock distribution across time servers, servers, SmartNICs, DPUs and high-speed network fabrics.

IEEE 1588 / PTP + PHC + GNSS Holdover + PCIe + SmartNIC / DPU + AI / HPC

Time Servers

Servers / Accelerators

SmartNIC / DPU

Leaf / Spine Fabric

PCIe / CXL

400G / 800G / 1.6T

Engineering Focus

A data-center platform contains a precision-time path for UTC traceability and timestamping, together with local low-jitter clock trees for PCIe, Ethernet, FPGA, SerDes and optical interfaces.

Selection Approach

Select each component from the receiving clock node: function, frequency, output logic, phase-noise or jitter definition, stability, holdover, temperature and board topology. Interface line rate alone is not an oscillator specification.

10 MHz

Time appliance, GNSSDO and holdover reference.

100 MHz

PCIe common-reference family.

125 / 156.25

Ethernet, SmartNIC, switch and SerDes nodes.

312.5 / 625

Device-specific FPGA and optical references.

01

One Infrastructure, Two Clock Domains

Data-center infrastructure combines a traceable precision-time path with independent low-jitter reference-clock domains.

Application definition: data centers, cloud platforms, AI/HPC and distributed-computing infrastructure that must maintain precise time across servers and network interfaces while supplying low-jitter reference clocks to high-speed I/O and fabric devices.

Representative Equipment

- PTP time server
- Grandmaster
- Rack server
- AI / HPC server
- NIC / SmartNIC
- DPU / IPU
- Accelerator card
- FPGA platform
- ToR / leaf switch
- Spine / fabric switch
- DCI equipment
- Storage / compute node

Applicable FCom Device Classes

Low-Jitter Differential XO

OCXO

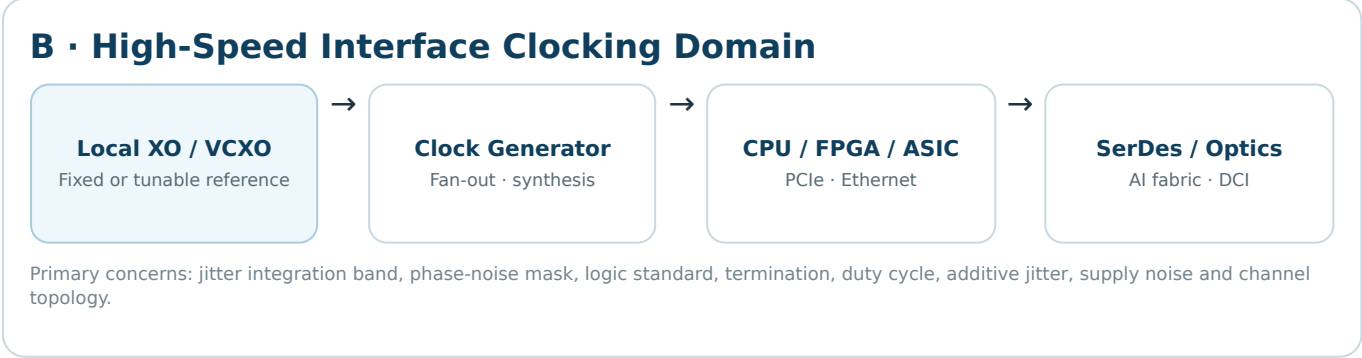
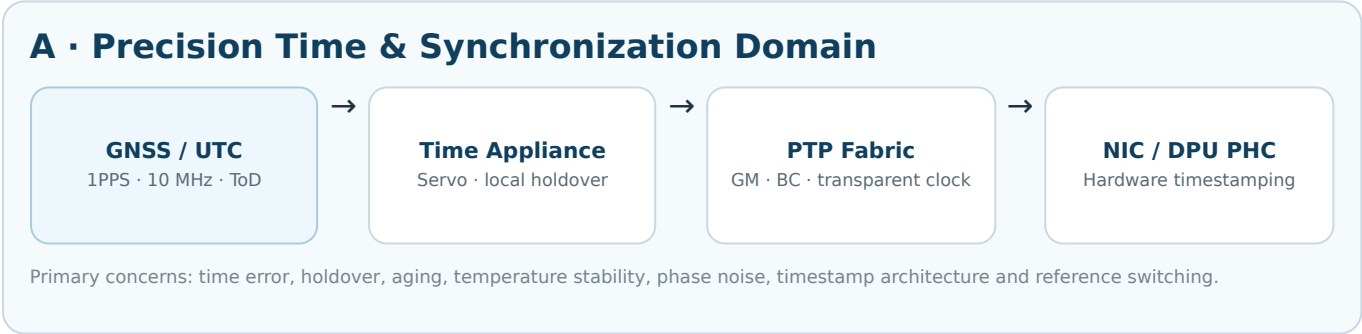
High-Stability TCXO

VCXO

CMOS XO

32.768 kHz Crystal / XO

Application-specific components: crystal filters, SAW filters and SAW resonators are outside the primary precision-time and digital reference-clock paths shown here. Where a platform includes a separately defined RF/IF path, FCom can evaluate the applicable filtering requirement as an additional design scope.



Keep the domains separate: an OCXO selected for time-server holdover and a differential XO selected for a PCIe or SerDes reference solve different problems. “800G” or “1.6T” describes aggregate data rate—not a discrete oscillator frequency.

02

Start with the Clock Node, Then Select the Device

The same rack may contain an OCXO, TCXO, differential XO, VCXO, CMOS oscillator and 32.768 kHz device. The correct selection follows the function and ownership of each clock node.

System Node	Clock Function	Representative Frequency	Recommended Device Class	Selection Focus
PTP Grandmaster / Time Server / Time Card	UTC-referenced time, local discipline and holdover during GNSS or upstream reference loss	10 MHz continuous reference; commonly paired with 1PPS and ToD	OCXO for stronger holdover; high-stability TCXO where size and power dominate.	PPB stability, aging, warm-up, phase noise, airflow sensitivity, servo method and permitted time error
NIC / SmartNIC / DPU PHC	Hardware timestamping, PHC discipline and PTP endpoint / boundary-clock operation	Device-defined local time core plus PCIe and Ethernet references	Treat PTP functionality and local clock selection as separate design decisions. Confirm the published clock pins and clocks generated on-card.	PHC architecture, PPS support, timestamp path, reference ownership, reset behavior and firmware discipline
CPU / PCIe Root Complex / Accelerator	PCIe reference distribution across root complex, retimer and endpoint	100 MHz common reference family	Use a low-jitter differential XO where the topology requires a discrete source; retain the defined common clock or generator in distributed-clock architectures.	Common-clock vs independent topology, SSC requirement, PCI-SIG jitter mask, termination and fan-out loading
Leaf / Spine Switch ASIC & Ethernet PHY	Core, TimeSync, management and SerDes reference clocks	12.8 / 20 / 25 / 32 / 50 / 100 / 125 / 156.25 MHz, device dependent	Use a low-jitter differential XO for exposed SerDes nodes; select a TCXO or CMOS XO where the target clock domain requires local stability or single-ended logic.	Separate timing/core/PCIe/SerDes domains, logic level, jitter band, supply noise and receiver termination
FPGA / SerDes / Optical / AI Fabric	High-speed transceiver and optical-interface reference	156.25 / 312.5 / 625 MHz are public device examples	Fixed differential XO selected against the configured transceiver PLL and its phase-noise mask.	Transceiver PLL, device phase-noise mask, electrical input limit, layout, coupling and clock switching
BMC / RTC / Low-Power Management	Timekeeping, telemetry, boot and standby management	32.768 kHz; controller frequencies such as 20 / 24 / 25 / 50 MHz	Passive tuning-fork crystal when the controller includes an oscillator circuit; low-current CMOS oscillator when an active clock is required.	Active vs passive architecture, CL, ESR, drive level, startup margin, standby current and temperature

1 · Identify the function

Holdover, timestamping, fixed REFCLK, pullable recovery, control or RTC.

2 · Confirm clock ownership

Discrete oscillator, common generator, recovered clock, DPPLL output or internal PLL.

3 · Define the interface

CMOS, clipped sine, rectangular, LVDS, LVPECL or HCSL with termination.

4 · Match the real metric

Stability/holdover for time; jitter/phase noise for high-speed I/O.

03

Representative Frequencies—Interpreted by Function

Interpret recurring frequencies by clock function, source ownership, interface topology and the receiving device's published limits.

Frequency / Clock-Plan Status	Typical Position	Device Guidance	Engineering Interpretation
1PPS / ToD Timing interface	GNSS receiver, time server, Time Card, timing I/O and PHC measurement	Timing interface—not a discrete oscillator frequency	1PPS transfers phase/time; ToD carries time-of-day data. They normally coexist with a continuous clock and a local disciplined oscillator.
32.768 kHz Local reference	BMC, RTC, standby controller and management domain	Passive tuning-fork crystal or low-current active CMOS clock	Choose the implementation from the controller circuit. Confirm CL, ESR and drive level for a passive crystal, or current, voltage and enable behavior for an active clock.
10 MHz Precision-time anchor	PTP grandmaster, GNSSDO, time appliance, external time I/O and local holdover	OCXO for stronger holdover; high-stability TCXO where size and power dominate	Prioritize aging, ppb stability, close-in phase noise, warm-up, power and thermal environment. The system servo and permitted time error determine the choice.
12.8 / 20 / 25 / 32 / 50 MHz Device-defined	Switch core, TimeSync/BroadSync, DPLL, management and controller references	TCXO, CMOS XO or differential XO according to input logic and time function	Public switch devices expose different requirements for core, synchronization and management clocks. The same frequency can require a different logic standard or jitter band.
100 MHz High-speed reference	PCIe common REFCLK, root complex, retimer and endpoint distribution	Fixed low-jitter HCSL or other receiver-compatible differential source when a discrete XO is appropriate	Confirm common-clock vs independent topology, SSC and the applicable PCIe jitter mask. A 100 MHz board node may be generated by a clock device rather than a dedicated XO.
125 MHz Architecture-dependent	Ethernet PHY, MAC, NIC and switch management / interface clocks	Low-jitter differential XO or CMOS XO, selected according to the target-device input	Frequency alone does not define the output logic. Confirm whether the PHY accepts an external oscillator, passive crystal, synthesized clock or recovered reference.
156.25 MHz Key differential point	Ethernet SerDes, SmartNIC, switch ASIC, FPGA and optical interface reference	Low-jitter differential XO; confirm LVDS, LVPECL or HCSL and the applicable jitter band	Use the target device's jitter band or phase-noise mask. Confirm receiver swing, termination, coupling and whether the clock is distributed through a buffer.
312.5 MHz Frequency fit; verify mask	FPGA transceiver, DSP and higher-rate electrical / optical interface	Higher-frequency differential XO with approved phase-noise evidence	A general jitter value does not by itself establish compliance with a device-specific offset-frequency mask. Phase-noise review is required.
625 MHz Device-specific	Selected high-speed FPGA and next-generation optical / AI-fabric reference inputs	External differential reference for target-device configurations that expose and specify this input	Some devices synthesize this frequency internally; others expose it as a reference option. Confirm the actual pin, interface limit and phase-noise mask before assigning an XO.

Reference basis: PCI-SIG documents the 100 MHz common-clock architecture; Broadcom BCM56980 publishes distinct 25/50 MHz timing, 100 MHz PCIe and 156.25 MHz SerDes references; AMD Versal Premium publishes transceiver phase-noise masks at 156.25, 312.5 and 625 MHz. Final clock assignments follow the selected device and board architecture.

04

Representative Platform & Architecture Matrix

Four public examples illustrate time appliances, SmartNIC / DPU timing, leaf-spine switching and high-speed FPGA reference clocks.

01 OCP TIME APPLIANCES PROJECT • TIME APPLIANCES Open Time Server / Time Card

Published platform information: the open PCIe Time Card architecture combines GNSS, a high-stability holdover oscillator, FPGA-based timing functions and host-visible PHC/PPS interfaces.

GNSS / 1PPS

Holdover Clock

FPGA / PHC

PTP / Host

Physical interface PCIe card;
Linux PHC and PPS exposure

External timing 1PPS / 10 MHz
SMA input and output

Resilience concept High-stability local oscillator bridges GNSS loss

Architecture lesson Traceability, holdover and host timestamping are separate functions

FCom engineering guidance: evaluate the local oscillator against the calculated holdover interval, aging, thermal profile and phase-noise budget. FCom can review a candidate series for a specific Time Card implementation after reviewing the schematic and control interface.

02 NVIDIA • SMARTNIC / DPU TIMING BlueField-3 DPU

Published platform information: BlueField-3 incorporates a PHC and supports PTP timing roles. Selected boards expose PPS input/output; NVIDIA documents that PTP is supported across BlueField DPUs while PPS and SyncE depend on hardware capability.

Network PTP

Hardware Timestamp

DPU PHC

Host / Workload

Clock roles Subordinate, master and boundary clock

PPS Available on selected BlueField-3 boards

Software path PTP stack, phc2sys and hardware timestamping

Qualification boundary Public timing information does not fully define every on-board oscillator requirement

FCom engineering guidance: evaluate the PHC/time domain separately from PCIe and Ethernet references. FCom can recommend a series after the board clock pins, logic standards and on-card clock generation are confirmed.

03 BROADCOM • LEAF / SPINE SWITCHING BCM56980 • 12.8 Tb/s Multilayer Switch

Published platform information: the device separates core, TimeSync, BroadSync, PCIe and SerDes reference-clock domains, demonstrating why one switch ASIC can require several unrelated clock specifications.

25 / 50 MHz TimeSync

100 MHz PCIe

156.25 MHz SerDes

Packet Fabric

BroadSync options 12.8 / 20 / 25 / 32 / 50 MHz

PCIe reference 100 MHz; 1.0 ps max for Gen3, 10 kHz–1.5 MHz

SerDes reference 156.25 MHz; 0.3 ps max, 12 kHz–20 MHz

Architecture lesson Clock-domain specifications must be evaluated independently

FCom engineering guidance: use the published input conditions for each clock domain. A low-jitter differential oscillator may fit the exposed SerDes node, while a separate device or buffer architecture may serve PCIe or TimeSync.

04 AMD • FPGA / HIGH-SPEED TRANSCEIVER Versal Premium GTY / GTYP

Published platform information: Versal Premium specifies a 60–820 MHz transceiver reference-clock range and publishes explicit oscillator phase-noise masks at 156.25, 312.5 and 625 MHz.

Differential XO

MGTREFCLK

GTY / GTYP PLL

SerDes / Optics

156.25 MHz mask -112 / -128 / -145 dBc/Hz at 10 kHz / 100 kHz / 1 MHz

312.5 MHz mask -103 / -123 / -143 dBc/Hz

625 MHz mask -98 / -117 / -140 dBc/Hz

Input context Differential MGTREFCLK; exact device configuration controls applicability

FCom engineering guidance: use frequency coverage as the initial screening criterion, then compare the approved oscillator phase-noise data with the selected GTY/GTYP PLL mask before qualification.

Reference scope: These public platforms are included to illustrate representative timing and interface architectures. FCom recommendations are made independently after review of the customer's actual clock tree, target device and operating requirements.

05

Traceable Time with Controlled Degradation

A resilient data-center timing path qualifies the external source, disciplines a local oscillator, distributes PTP through the fabric and aligns host or accelerator clocks through PHC-aware software.

LAYER 1 External References

GNSS / UTC

1PPS · 10 MHz · ToD

Upstream PTP → Local Policy

Network time source · Qualification
and alarms

Qualify the reference first

Source quality, antenna path, asymmetry, leap-second handling and failure mode determine the downstream timing strategy. Timing interfaces—not oscillator frequencies

LAYER 2 Time Appliance

DPLL / Servo

Phase and frequency control

Local Holdover → GM Outputs

OCXO or high-stability TCXO · PTP ·
1PPS · 10 MHz

Select from the holdover budget

An OCXO supports designs where aging, time error and close-in noise dominate. A high-stability TCXO supports size- and power-sensitive designs when the calculated holdover budget allows. 10 MHz class · verify servo/control method

LAYER 3 Network Distribution

Grandmaster

PTP source

Leaf / Spine → NIC / DPU PHC

BC / TC or PTP-aware fabric ·
Hardware timestamp endpoint

Add pullability where required

An external VCXO is appropriate when the selected DPLL or recovery loop specifies a pullable reference. Confirm APR, gain, control voltage and loop bandwidth

LAYER 4 Host & Workload

PHC

NIC / DPU hardware clock

System Clock → Application

phc2sys / equivalent · Database ·
storage · AI/HPC

Measure the end-to-end path

Timestamp hardware, firmware, OS servo, network asymmetry and application clock access can dominate the final time error. Combine oscillator quality with system-level validation

Holdover device trade-off

Long holdover / low aging: OCXO
Compactness / lower power: TCXO
Closed-loop pullability: VCXO

Minimum holdover calculation inputs

Initial accuracy · temperature profile · aging · retrace · supply sensitivity · airflow and thermal transients · time without valid reference · permitted frequency/phase/time error · calibration interval · servo estimator and recovery behavior.

A $\pm$ ppb value alone does not define achievable holdover time. Calculate the full error budget and validate it under the intended airflow and thermal profile.

06

Three High-Speed Clocking Architectures

Server, SmartNIC, network-fabric and optical-interconnect nodes use different clock-distribution and transceiver-reference architectures.

SERVER / ACCELERATOR

PCIe Root Complex, Retimer and Endpoint

1. 100 MHz common REFCLK or independent architecture
2. Clock generator / fan-out
3. CPU / GPU / accelerator / retimer
4. PCIe link and CXL-capable platform path

Design check: identify whether the platform uses a common clock, clock generator, separate reference or data-clocked architecture before assigning an XO.

SMARTNIC / DPU / SWITCH

PHC, Packet Timing and Ethernet SerDes

1. PTP packets / PPS
2. Hardware timestamp + PHC
3. Switch ASIC / NIC / DPU clock tree
4. 125 / 156.25 MHz-class Ethernet references

Design check: logic level, termination, additive jitter, phase-noise band, source/load placement and clocks already synthesized on-card.

AI FABRIC / FPGA / OPTICAL DCI

Higher-Frequency Transceiver References

1. Fixed differential XO
2. 156.25 / 312.5 / 625 MHz reference
3. FPGA / DSP transceiver PLL
4. 800G / 1.6T optics or scale-out fabric

Design check: high-frequency coverage is not equivalent to mask compliance. Review offset-frequency noise, clock coupling, input amplitude, package and routing loss.

PCIe Root Complex, Retimer and Endpoint — Selection Gate

Device choice: a fixed low-jitter differential XO may be considered where the topology calls for a discrete source. Confirm the PCIe jitter mask, SSC policy, receiver interface and fan-out architecture.

PHC, Packet Timing and Ethernet SerDes — Selection Gate

Device choice: a low-jitter differential XO may be considered for an exposed 125 or 156.25 MHz SerDes node. Keep PHC discipline, PCIe REFCLK and Ethernet references as separate decisions.

Higher-Frequency Transceiver References — Selection Gate

Device choice: evaluate a low-jitter differential XO at 156.25 MHz; above that range, confirm both frequency coverage and approved phase-noise evidence for the configured transceiver PLL.

Layout guidance: place the lowest-jitter source close to the consuming IC or clock buffer, maintain the specified differential impedance, isolate switching-regulator noise, minimize stubs, control the return path and confirm whether termination is inside the source, buffer or receiver.

07

Four Decisions Where a Series Selection Matters

The representative FCom series below address four decisions where stability class, pullability, output format or usable frequency range materially affects the design.

Decision 1 • 10 MHz-class holdover: performance vs size and power

FOC-5S-LN / FVT-7S-HP

OCXO option: 14×9 SMD · 10–40 MHz · ±5 ppb · -40 to +85°C

TCXO option: 7050 SMD · 5–52 MHz · ±50 ppb · -40 to +105°C

Key boundary: Holdover, aging and close-in noise versus footprint, power and warm-up

The OCXO option may be considered where holdover or close-in phase noise dominates. The TCXO option supports a lower-power architecture when the calculated time-error budget allows.

Decision 2 • Exposed 100 / 125 / 156.25 MHz differential node

FCO-3L-UJ

Range / Output: 100–220 MHz · LVPECL / LVDS / HCSL · 1.8 / 2.5 / 3.3 V

Environment: 3225, 6-SMD · ±20 ppm · -40 to +125°C

Key boundary: 50 fs series jitter value; confirm band, SSC, interface and mask

This series is a representative review starting point when the target architecture exposes a discrete low-jitter differential reference within this range.

Decision 3 • External pullable clock in a DPLL or recovery loop

FVC-3P-LJ

Range / Output: 10–250 MHz · CMOS · 2.5 / 3.3 V

Control / Temp.: ±50 to ±150 ppm pull options · -40 to +105°C

Key boundary: For timing ICs that specify an external pullable VCXO reference

This series supports DPLL and recovery-loop architectures requiring an external VCXO. Confirm APR, control voltage, gain, linearity and loop phase-noise transfer.

Decision 4 • Device-specific 312.5 / 625 MHz reference

FCO-3L-PG

Range / Output: 10–1500 MHz · LVPECL / LVDS · 2.5 / 3.3 V

Environment: 3225, 6-SMD · ±25 ppm · -40 to +105°C

Key boundary: 0.6 ps series jitter value; confirm the applicable phase-noise mask

This series provides frequency coverage above 220 MHz. Final selection should be confirmed against the configured FPGA, DSP or SerDes phase-noise mask.

1 • Define the Node

Holdover, fixed differential reference, pullable recovery loop or device-specific high-frequency input.

2 • Confirm the Interface

Supply, output logic, receiver swing, termination, enable behavior and clock-input topology.

3 • Set the Performance Budget

Stability, aging, phase noise, RMS-jitter integration band, pull range and holdover interval.

4 • Finalize the Configuration

Package, temperature range, qualification, test conditions, ordering code and sample-validation plan.

Ordering note: Codes shown are FCom series identifiers from the current product portfolio. FCom confirms the final orderable configuration against frequency, supply, output logic, enable/standby function, stability, temperature, package, pull range and agreed measurement conditions.

08

Validate the Clock Path, Not Only the Frequency

Confirm the complete clock path, electrical interface, jitter or phase-noise definition and time-error budget before requesting a configuration.

Primary Technical Requirements

Validation Item	What to Confirm
Clock-node function	Holdover, PHC discipline, hardware timestamping, fixed REFCLK, tunable recovery, controller crystal or RTC.
Clock ownership	Discrete oscillator, common generator, recovered reference, DPLL output, internal PLL or clock delivered across the connector.
Output interface	CMOS, clipped sine, rectangular, LVDS, LVPECL or HCSL; amplitude, common mode, coupling and termination.
Jitter / phase noise	Integration band, offset-frequency mask, additive jitter, SSC state, test fixture and measurement conditions.
Time performance	PTP profile, timestamp point, network asymmetry, time-error budget, holdover interval and reference switching.
Environment	Operating temperature, airflow, thermal ramp, supply noise, shock/vibration, altitude and qualification requirements.
Layout / SI	Impedance, source/load termination, trace length, stubs, crosstalk, return path, fan-out loading and decoupling.
Lifecycle	Prototype quantity, annual usage, production date, change control, traceability and second-source policy.

Minimum RFQ Information

Electrical

- Exact frequency and tolerance
- Supply voltage
- Output logic / load
- OE / standby behavior
- Rise/fall and duty cycle

Timing Performance

- RMS jitter and band
- Phase-noise mask
- Stability and aging
- Holdover target / time error
- Pullability / control voltage

Mechanical / Environmental

- Package and height
- Temperature and airflow
- Reflow profile
- Shock/vibration
- Compliance / qualification

Platform / Program

- Target IC and clock pin
- Schematic / clock tree
- PTP / PCIe / SerDes topology
- Prototype, EAU and schedule
- Approved-vendor requirements

Request an Application Review

Please share the clock tree, target-device data sheet and required timing limits. FCom application engineering will review each clock node, recommend the appropriate device family and confirm whether a standard or customized configuration is required.

[Technical Review](#)
[General RFQ](#)

Recommended submission: annotate every oscillator, crystal or clock-generator input on the block diagram with node name, target pin, frequency, output type, timing limit and ownership of the reference.

09

Engineering FAQ & Technical References

Common data-center timing questions, public technical references and the information required for FCom application review.

Does PTP remove the need for a local oscillator?

No. PTP transfers time across the network, while each time appliance, NIC, DPU and switch still depends on a local clock. Its phase noise, stability and holdover behavior affect the final result.

Is every PCIe reference clock a discrete 100 MHz XO?

No. It may be distributed from a common generator, provided locally or implemented through another allowed topology. Evaluate a discrete XO after confirming the platform clock architecture.

Can 156.25 MHz be selected from Ethernet port speed?

No. It is a common reference point, but the exact frequency, logic and jitter requirement come from the configured ASIC, PHY, FPGA or SerDes input—not the advertised port rate.

Does tighter stability imply lower jitter?

No. Stability describes long-term and environmental frequency error; jitter and phase noise describe short-term timing fluctuation. They are different specifications and often dominate at different nodes.

When should an OCXO replace a TCXO?

When the holdover duration, aging, thermal profile or phase-noise target exceeds the TCXO error budget. The decision should follow a quantified time-error and holdover calculation.

When are 312.5 or 625 MHz external references?

They are used when the selected FPGA, DSP or SerDes configuration exposes and specifies such an input. Many platforms synthesize higher internal clocks from a lower-frequency external reference.

Selected Public Architecture & Frequency Sources

1. OCP Time Appliances Project · Time Card and Open Time Server—PCIe time-card architecture, PHC/PPS exposure, 1PPS / 10 MHz interfaces and local holdover concept.
2. NVIDIA BlueField-3 Supported Interfaces and DOCA Firefly Service—PHC, PTP roles and hardware-dependent PPS / SyncE capabilities.
3. Broadcom BCM56980 Data Sheet—core, TimeSync, BroadSync, PCIe and SerDes reference frequencies, tolerance and jitter bands.
4. AMD Versal Premium GTY / GTYP Reference Clock Characteristics and Phase-Noise Mask—60–820 MHz range and 156.25 / 312.5 / 625 MHz masks.
5. PCI-SIG PCIe 5.0 System Implementation Q&A—100 MHz Common REFCLK architecture across root complex, retimer and endpoint.
6. IEEE 1588-2019—Precision Clock Synchronization Protocol for Networked Measurement and Control Systems.

Platform reference notice: Third-party platform names and published specifications are included for architecture reference only. Their inclusion does not imply adoption, certification, compatibility, endorsement or pin-to-pin replacement.

FCom APPLICATION ENGINEERING

Turn Your Clock Tree into a Qualified BOM

Share the system node, target IC, frequency, output logic, jitter/phase-noise target, stability/holdover requirement, temperature range and program quantities. FCom application engineering will recommend the appropriate series and confirm the configuration for quotation and sample validation.

Product parameters in this guide represent performance ranges from the current FCom product portfolio. Final specifications and orderable configurations are confirmed through FCom application review, quotation and approved product documentation.

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