

CARRIER TIMING · PACKET CLOCKING · OPTICAL TRANSPORT · BROADBAND ACCESS

Carrier Transport, Switching & Access Networks

Preserve network synchronization and low-jitter reference clocking across carrier routing, switching, optical transport and broadband-access infrastructure.

PTP / IEEE 1588 + SyncE + Holdover + OTN / WDM + Carrier Ethernet + xPON / OLT

Core / Edge Routing

Carrier Ethernet

OTN / WDM

Fronthaul / Backhaul

xPON / OLT

Timing Cards

SerDes REFCLK

Engineering Focus

A carrier platform commonly contains two clock systems: a traceable network-synchronization chain and a local low-jitter clock tree for switch ASICs, PHYs, FPGAs, SerDes and optical interfaces.

Selection Approach

Select each component from its receiving clock node. Frequency, output logic, jitter band, phase noise, stability, holdover, pull range, temperature and qualification should be confirmed before the ordering configuration is finalized.

10 MHz

PRTC, grandmaster and holdover reference.

19.44-155.52 MHz

Telecom transport and recovered-clock families.

156.25 MHz

Key high-speed differential reference point.

312.5 MHz+

Device-specific references requiring jitter validation.

01

One Platform, Two Clock Domains

Carrier platforms combine traceable network synchronization with independent low-jitter data-clock domains.

Application definition: carrier core, aggregation and access equipment—including routers, switches, OTN/WDM systems and broadband-access platforms—that must transport traceable network timing while maintaining low-jitter local clocks for high-speed data interfaces.

Representative Equipment

- Core / edge routers
- Cell-site routers
- Carrier Ethernet switches
- Aggregation switches
- OTN / PTN equipment
- WDM / ROADM systems
- Coherent optical shelves
- Packet muxponders
- xPON OLT / ONU
- Broadband access nodes
- Line cards
- Timing / control cards

Applicable FCom Device Classes

Differential XO

Low-Jitter XO

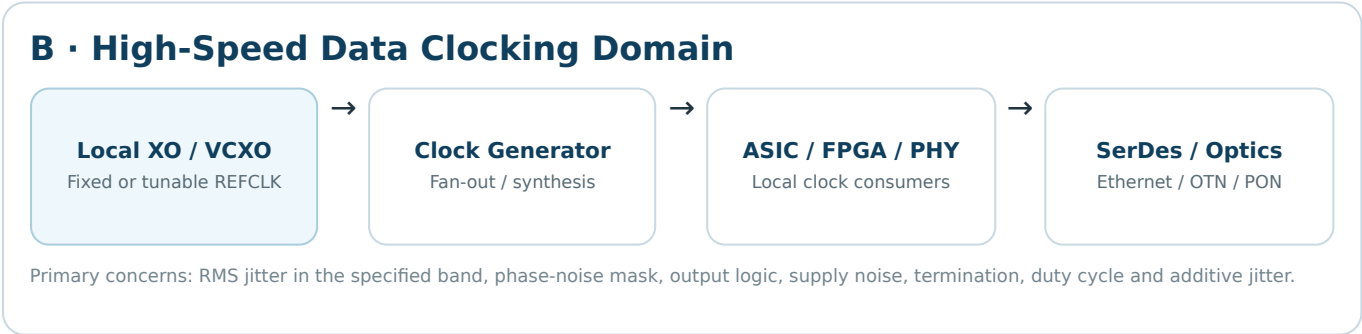
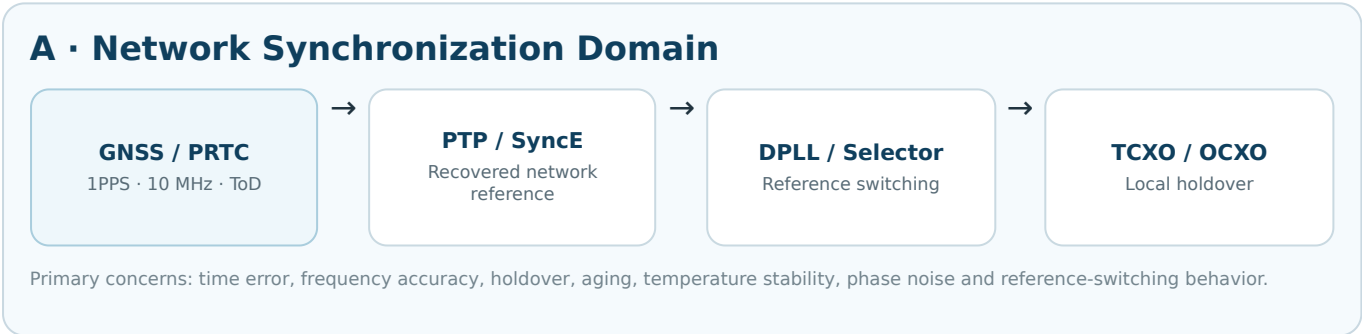
VCXO

TCXO

OCXO

Quartz Crystal

Application-specific components: SAW filters, SAW resonators and MCF crystal filters are not primary timing devices in this architecture. They may be considered when the equipment includes a defined RF/IF receiver or fixed-wireless radio path.



Keep clock-domain specifications separate: a ± 5 ppb OCXO may be selected for holdover, while a 50 fs differential XO may be selected for a SerDes reference. These parameters describe different design objectives, and a 100G/400G line rate is not an oscillator frequency.

02

Start with the Clock Node, Then Select the Device

The same carrier chassis may use an OCXO, TCXO, VCXO, differential XO, CMOS XO and passive crystal. The correct choice follows the function of each clock node.

System Node	Clock Function	Representative Frequency	Recommended Device Class	Selection Focus
PRTC / PTP Grandmaster / Timing Card	Traceable local reference and holdover when GNSS or network timing is unavailable	10 MHz; commonly paired with 1PPS and ToD interfaces	Low-noise OCXO for long holdover; high-precision TCXO when size and power dominate	ppb stability, aging, warm-up, holdover, phase noise, power and airflow sensitivity
SyncE / PTP Boundary Clock	Recover, filter, select and redistribute frequency / phase / time	10 / 19.44 / 25 / 38.88 / 51.84 MHz and DPLL-defined references	High-precision TCXO or pullable VCXO/VCTCXO, according to the loop function	stability vs holdover interval, pull range, loop bandwidth, wander and phase-noise transfer
Switch ASIC / Ethernet PHY / SerDes	Low-jitter local differential REFCLK	25 / 50 / 100 / 125 / 156.25 / 312.5 MHz, device dependent	Low-jitter differential XO; wide-frequency XO only after jitter qualification	LVDS/LVPECL/HCSL, integration band, additive jitter, termination and power-supply noise
OTN Framer / Muxponder / Coherent DSP	Telecom-rate clock recovery, synthesis and high-speed optical reference	19.44 / 38.88 / 77.76 / 155.52 / 311.04 / 622.08 MHz	VCXO for recovery loops; low-jitter differential XO for fixed REFCLK nodes	fixed vs tunable reference, close-in phase noise, jitter transfer, logic level and DSP-specific mask
OLT / PON Line Card / Ethernet Uplink	System synchronization plus local PON/Ethernet PHY clocking	19.44 / 25 MHz inputs; 25 / 125 / 156.25 MHz outputs are public reference-design examples	High-stability timing reference plus separate CMOS or differential PHY clocks	separate timing chain from PHY clock tree; validate the PON chipset and line-card clock plan
CPU / BMC / FPGA Control / RTC	Management, boot, telemetry and low-power timekeeping	32.768 kHz; 10 / 20 / 24 / 25 / 40 / 50 MHz, controller dependent	Passive crystal, CMOS XO or 32.768 kHz crystal/oscillator as required by the controller	startup margin, CL/ESR, current, temperature, standby behavior and controller oscillator drive

1 · Identify the node

Holdover, recovery, synthesis, SerDes reference, control or RTC.

2 · Confirm the frequency source

Board oscillator, recovered line clock, DPLL output or internal synthesis.

3 · Define the output

CMOS, clipped sine, sine, LVDS, LVPECL or HCSL with termination.

4 · Match the real metric

Stability/holdover for synchronization; jitter/phase noise for data conversion and SerDes.

03

Representative Frequencies—Interpreted by Function

Interpret recurring frequencies by clock function, source ownership and the requirements of the receiving interface.

Frequency / Clock-Plan Status	Typical Position	Device Guidance / FCom Series	Engineering Interpretation
1PPS / ToD Timing interface	GNSS receiver, PRTC, grandmaster, timing I/O	Timing interface—not a discrete oscillator frequency	1PPS transfers phase/time; ToD carries time-of-day data. They normally coexist with a continuous reference such as 10 MHz.
32.768 kHz Local reference	BMC, RTC, low-power control domain	Passive tuning-fork crystal or low-current CMOS oscillator	Use a passive crystal when the controller provides the oscillator circuit; an active clock may be considered where required by the system architecture.
10 MHz Synchronization anchor	PRTC, PTP grandmaster, GNSSDO, external timing I/O	OCXO for long holdover; TCXO where size and power dominate	Prioritize aging, ppb stability and close-in phase noise. Holdover performance should be calculated from the complete oscillator and control-loop specification before a series is selected.
8 kHz / 1.544 / 2.048 MHz Usually recovered	Legacy telecom synchronization inputs	Recovered or synthesized; use a local XO only when specified	Synchronizer data sheets commonly accept these rates as inputs; this does not imply a dedicated board oscillator at each frequency.
19.44 / 38.88 / 51.84 MHz Stable or tunable reference	SDH/SONET/OTN synchronization, line cards and timing cards	High-precision TCXO for local stability; VCXO/VCTCXO for closed-loop recovery	TCXO supports local stability/holdover; VCXO supports pulling in a recovery loop. Verify output waveform and DPLL control range.
25 / 50 / 62.5 MHz Local reference	Controllers, Ethernet PHYs, switch clock trees and PON line cards	CMOS XO, differential XO or passive crystal according to the target IC	Select active XO or passive crystal from the target device oscillator circuit. Differential logic is not implied by frequency alone.
100 / 125 MHz High-speed reference	Ethernet PHY, switch ASIC, FPGA, PCIe/SerDes management domains	Low-jitter differential XO; CMOS XO when specified by the target device	Confirm the required logic level and jitter band, as 100/125 MHz clock inputs may use different output standards.
155.52 / 156.25 MHz Key differential point	OTN/SDH clocking; 10G/25G/100G-class Ethernet and SerDes references	Representative 100-220 MHz low-jitter differential XO class — representative FCom 3225 low-jitter differential XO class	100–220 MHz, LVDS/LVPECL/HCSL, ± 20 ppm, -40 to $+125^{\circ}\text{C}$ and 50 fs RMS jitter. Confirm the applicable integration band in the approved specification.
311.04 / 312.5 MHz Frequency fit; verify jitter	OTN clock synthesis, higher-rate SerDes and optical interface references	Representative wide-frequency differential XO class for higher-frequency reference nodes	The series covers frequencies up to 1500 MHz with 0.6 ps RMS jitter. Final qualification is based on the target-device jitter mask and integration band.
622.08 MHz and higher Device-specific	High-order transport clocks, DSP/SerDes references or internally synthesized nodes	Application review required before assigning an external oscillator	Many platforms synthesize these frequencies internally. An external oscillator is selected when the target IC provides and specifies the corresponding reference input.

Engineering reference basis: Microchip DS3106 and ZL30145 document telecom and Ethernet timing families; Microchip ZL30721 shows 19.44/25 MHz timing-card inputs and 25/125/156.25 MHz outputs for OLT/ONU/DSLAM-class equipment; Broadcom BCM56980 documents switch-device reference-clock options. These frequencies illustrate common architectures; final clock assignments remain device- and platform-specific.

04

Representative Platform & Architecture Matrix

Four public examples illustrate core switching, access routing, OTN / FlexE and PON / DSLAM timing architectures.

BROADCOM · CORE / AGGREGATION SWITCHING

01

BCM56980 · Tomahawk 3 Multilayer Switch

Published platform information: 12.8 Tb/s switching with up to 32×400GbE, 64×200GbE or 128×100GbE. The data sheet identifies separate core, TimeSync, BroadSync, PCIe and SerDes reference-clock domains.

50 MHz Core

25 / 50 MHz TimeSync

100 MHz PCIe

156.25 MHz SerDes

Core reference 50 MHz · ±50 ppm · 10 ps RMS, 12 kHz–20 MHz

PCIe reference 100 MHz · ±300 ppm · 1.0 ps RMS for Gen3, 10 kHz–1.5 MHz

SerDes reference 156.25 MHz · ±50 ppm · 0.3 ps RMS, 12 kHz–20 MHz

Network timing Integrated IEEE 1588v2 and SyncE; BroadSync accepts 12.8 / 20 / 25 / 32 / 50 MHz

FCom engineering guidance: evaluate synchronization, PCIe and low-jitter SerDes reference nodes independently, as each domain has different electrical and timing requirements.

CISCO · CARRIER ACCESS / AGGREGATION ROUTING

02

NCS 540 Medium Density Series

Published platform information: carrier routers with 1/10/25/40/100GbE options, SyncE, IEEE 1588 PTP and—on selected variants—an internal GNSS receiver. Timing interfaces vary by SKU.

GNSS / External Source

1PPS · 10 MHz · ToD

PTP / SyncE / BITS

Packet Interfaces

Timing roles T-GM, T-BC and T-TSC

Profiles G.8265.1 · G.8275.1 · G.8275.2

Clock class G.8273.2 Class B / C, model dependent

Published scope System-level timing I/O is published; the internal oscillator BOM is platform-specific

FCom engineering guidance: select the local reference from the required holdover interval, aging, temperature and phase-noise budget. System timing interfaces alone do not define the internal oscillator specification.

ALTERA · OTN / FLEXE FPGA INTERFACE

03

Agilex 7 E-Tile 10GE / 25GE Design Example

Published platform information: the public PCS-only, OTN or FlexE simulation design example reports a 322.265625 MHz reference clock, illustrating that the external clock follows the selected transceiver/IP mode rather than the nominal Ethernet port speed.

Client / Line Data

322.265625 MHz REFCLK

E-Tile PCS / RS-FEC

OTN / FlexE Path

Representative node FPGA-based optical transport or flexible Ethernet line card

Published frequency 322.265625 MHz in the cited design example

Architecture guidance Follow the generated IP configuration and device clocking requirements

Qualification boundary Confirm the jitter mask and board-level output interface for the selected configuration

FCom engineering guidance: at 322.265625 MHz, confirm frequency coverage together with the configured transceiver input limit, output interface and required jitter integration band.

MICROCHIP · TIMING CARD / OLT / ONU / DSLAM

04

ZL30721 Telecom Timing Card Reference Architecture

Published reference design: 19.44 / 25 MHz and other line-card inputs feed an IEEE 1588 / SyncE network synchronizer. The example generates two 156.25 MHz differential clocks plus 125 MHz and 25 MHz CMOS outputs.

19.44 / 25 MHz Inputs

DPLL / Holdover

2×156.25 MHz

125 / 25 MHz CMOS

Local reference TCXO or OCXO at ≥10 MHz

Output jitter As low as 0.25 ps RMS, 12 kHz–20 MHz, device dependent

Applications Edge router, access aggregation, EPON/GPON OLT/ONU/ONT and DSLAM

Architecture guidance Separate holdover stability from low-jitter output generation

FCom engineering guidance: identify the clocks synthesized by the DPLL before assigning separate holdover or fixed-XO positions. This avoids duplicating a clock already generated within the timing architecture.

Reference scope: These public platforms are included solely to illustrate representative timing and interface architectures. Their inclusion does not imply FCom content, qualification, compatibility or pin-to-pin replacement.

05

Traceable Timing with Controlled Degradation

A resilient carrier timing chain selects between GNSS, PTP, SyncE and external references, filters the selected source and uses a stable local oscillator to bridge reference loss.

LAYER 1 External References

GNSS / PRTC
1PPS · 10 MHz · ToD

PTP → SyncE
G.8275.1 / G.8275.2 · Recovered
physical-layer frequency

Define reference requirements before oscillator selection

First define priority, traceability, time-error budget and loss-of-reference behavior.
Reference interfaces ≠ oscillator frequency

LAYER 2 Synchronizer / DPLL

Reference Monitor
Validity · SSM/QL · PTP state

Clock Selector → DPLL
Hitless or controlled switching ·
Wander filtering · phase tracking

VCXO or controlled TCXO

Use a pullable CMOS or differential VCXO when the loop architecture requires tuning; select by loop frequency, output logic and pull range.
Available pullability options: ±50 to ±150 ppm

LAYER 3 Local Holdover

TCXO
Compact, lower power, shorter holdover

OCXO → Servo / Calibration
ppb stability and improved long holdover · Aging and temperature compensation

Select after holdover calculation

Compare initial accuracy, temperature error, aging, retrace, supply sensitivity and servo behavior against the permitted time-error budget.
TCXO for compactness · OCXO for stronger holdover

LAYER 4 Timing Distribution

PTP / T-BC
Packet phase and time

SyncE → 1PPS / 10 MHz
Physical-layer frequency · Local and external timing I/O

Validate output-clock consumers

The DPLL may synthesize multiple outputs; avoid adding an independent XO where the required clock is already generated and qualified.
Check wander, phase noise and output format

Holdover device trade-off

Long holdover / low aging: OCXO
Compactness / lower power: TCXO
Closed-loop pulling: VCXO

Minimum holdover calculation inputs

Initial accuracy · temperature profile · aging · retrace · supply sensitivity · airflow / thermal transient · duration without valid reference · permitted frequency/phase/time error · calibration interval · DPLL estimator behavior.

A complete holdover assessment is required; the ±ppb value alone does not define the achievable holdover time.

06

Three Data-Clocking Architectures

Routing, optical transport and broadband-access nodes use different recovery, synthesis and fixed-reference clock paths.

ROUTING & SWITCHING

Switch ASIC / PHY / SerDes Clock Tree

1. Local fixed differential XO
2. Clock generator / fan-out buffer
3. Switch ASIC · FPGA · Ethernet PHY
4. 25G / 100G / 400G electrical and optical ports

Design check: output logic, termination, integration band, additive jitter and supply filtering.

OPTICAL TRANSPORT / OTN

Recovery, Mapping and Coherent Interfaces

1. Client / line recovered clock
2. DPPLL + VCXO / local reference
3. OTN framer · muxponder · coherent DSP
4. ROADM / WDM line interface

Design check: 311.04/312.5/622.08 MHz references require verification against the applicable DSP jitter mask.

BROADBAND ACCESS / PON

OLT System Timing and Line-Card Clocks

1. Upstream PTP / SyncE reference
2. OLT timing card / boundary clock
3. Switch fabric + PON MAC/PHY + uplink SerDes
4. ODN → ONU / ONT / mobile endpoint

Design check: determine the board oscillator from the PON chipset and line-card clock plan rather than from the PON generation or downstream bit rate alone.

Switch ASIC / PHY / SerDes Clock Tree — Selection Gate

Selection anchor:
Representative 100–220 MHz low-jitter differential XO class at 100–220 MHz differential nodes, especially the common 156.25 MHz class. A general-purpose CMOS XO may be considered at lower-rate controller or PHY references.

Recovery, Mapping and Coherent Interfaces — Selection Gate

Selection anchor:
Representative pullable low-jitter CMOS VCXO class supports 10–250 MHz pullable CMOS reference nodes. For fixed low-jitter differential positions outside the tuning loop, select a differential XO.

OLT System Timing and Line-Card Clocks — Selection Gate

FCom application guidance:
A high-stability TCXO or OCXO may be considered for local timing, a low-jitter XO for exposed line-card interfaces, and a passive crystal only when required by the target chipset.

Layout guidance: position the lowest-jitter source close to the consuming IC, maintain the specified differential impedance, isolate noisy supplies and switching regulators, minimize stubs and confirm whether the clock device or target IC provides internal termination.

07

Four Application-Driven Selection Anchors

The following FCom series address four clock-node decisions where stability, frequency range, output logic or pullability materially affects device selection. Other positions can be finalized through FCom application review.

Holdover decision: performance vs size and power

FOC-5S-LN / FVT-7S-HP

OCXO option: OCXO · 14×9 SMD · 10–40 MHz · ±5 ppb

Noise / Temp.: -162 dBc/Hz @10 kHz · -40 to +85°C

TCXO option: TCXO · 7050 · 5–52 MHz · ±50 ppb

Output / Temp.: Clipped sine / CMOS · -40 to +105°C

The OCXO option may be considered when long holdover or close-in phase noise is the priority. The TCXO option may be considered where size and power are more important and the calculated holdover budget permits a TCXO.

156.25 MHz-class fixed differential reference

FCO-3L-UJ

Package / Range: 3225, 6-SMD · 100–220 MHz

Output / Supply: LVPECL / LVDS / HCSL · 1.8 / 2.5 / 3.3 V

Stability / Temp.: ±20 ppm · -40 to +125°C

RMS jitter: 50 fs

This series is a representative FCom starting point for an exposed 155.52 / 156.25 MHz differential node. Confirm output standard, receiver swing, termination and jitter integration band.

Pullable clock-recovery or DPLL node

FVC-3P-LJ

Package / Range: 3225, 6-SMD · 10–250 MHz

Output / Supply: CMOS · 2.5 / 3.3 V

Stability / Temp.: ±25 to ±50 ppm · -40 to +105°C

Pullability: ±50 to ±150 ppm options

This series may be considered when the recovery loop requires an external pullable CMOS reference. For fixed low-jitter differential nodes, evaluate an appropriate differential XO instead.

>220 MHz coverage for device-specific references

FCO-3L-PG

Package / Range: 3225, 6-SMD · 10–1500 MHz

Output / Supply: LVPECL / LVDS · 2.5 / 3.3 V

Stability / Temp.: ±25 ppm · -40 to +105°C

RMS jitter: 0.6 ps

This series provides frequency coverage for external reference nodes above 220 MHz. Final selection is confirmed against the target DSP or SerDes jitter mask and integration band.

1 • Define the Node

Holdover, fixed differential reference, pullable recovery loop or device-specific high-frequency input.

2 • Confirm the Interface

Supply, output logic, receiver swing, termination, enable behavior and clock-input topology.

3 • Set the Performance Budget

Stability, aging, phase noise, RMS-jitter integration band, pull range and holdover interval.

4 • Finalize the Configuration

Package, temperature range, qualification, test conditions, ordering code and sample-validation plan.

Configuration note: The series shown are representative selection anchors. The final ordering configuration is confirmed against frequency, supply voltage, output logic, enable function, stability, temperature range, package, pull range and agreed test conditions.

08

Validate the Clock Path, Not Only the Frequency

Confirm the complete clock path, electrical interface and timing budget before requesting a frequency-specific configuration.

Engineering Validation Checklist

Validation Item	What to Confirm
Clock-node function	Holdover, DPLL reference, fixed REFCLK, tunable recovery, controller crystal or RTC.
Frequency ownership	External oscillator, recovered clock, synchronizer output, clock generator or internal PLL.
Output interface	CMOS, clipped sine, sine, LVDS, LVPECL or HCSL; amplitude, common mode and termination.
Jitter / phase noise	Integration band, offset-frequency mask, additive jitter and measurement conditions.
Synchronization	PTP profile, SyncE, SSM/ESMC, time-error budget, holdover interval and reference switching.
Environment	Operating temperature, airflow, thermal ramp, shock/vibration, supply noise and qualification.
Layout	Impedance, source/load termination, trace length, stubs, crosstalk, return path and decoupling.
Lifecycle	Prototype quantity, annual usage, mass-production date, change control and second-source policy.

Minimum RFQ Data

Electrical

- Frequency and tolerance
- Supply voltage
- Output logic / load
- OE / standby behavior
- Rise/fall and duty cycle

Timing Performance

- RMS jitter and band
- Phase-noise mask
- Stability and aging
- Holdover target
- Pullability / control voltage

Mechanical / Environmental

- Package and height
- Temperature range
- Reflow profile
- Shock/vibration
- Compliance / qualification

Program

- Target IC and clock pin
- Schematic / clock tree
- Prototype and EAU
- Schedule and production site
- Approved-vendor requirements

Request an Application Review

Please share the clock tree, target-device data sheet and required timing limits. FCom application engineering will review each clock node, recommend the appropriate device family and confirm whether a standard or customized configuration is required.

[Technical Review](#)
[General RFQ](#)

Recommended submission: To support a faster application review, annotate each oscillator or crystal position on the block diagram with the node name, target pin, frequency, output type and timing limit.

09

Engineering FAQ & Technical References

Common carrier-network timing questions, public technical references and the information required for FCom application review.

Is 10 MHz the clock for every block in a synchronized router?

No. It is commonly a system timing reference. Switch ASICs, PHYs, SerDes and optical interfaces normally use separate local references or clocks synthesized by a clock device.

Can a 156.25 MHz oscillator be selected from the port speed?

No. It is a common Ethernet reference point, but the exact frequency and logic must come from the target ASIC/PHY/SerDes data sheet and board clock architecture.

Does lower frequency stability mean lower jitter?

No. Stability describes long-term and environmental frequency error; jitter and phase noise describe short-term timing fluctuations. Carrier systems often require both, at different nodes.

When should an OCXO replace a TCXO?

When the holdover duration, aging, temperature profile or phase-noise target exceeds the TCXO budget. The decision should follow a quantified holdover-error calculation.

When is a VCXO appropriate?

When a DPLL, clock-recovery or synchronization loop explicitly requires a pullable reference. Confirm control voltage, gain, APR/pull range, linearity and phase-noise transfer.

Are SAW and MCF products part of every carrier timing BOM?

Not typically. They are application-specific RF/IF filtering components used when the equipment includes a defined radio receiver, fixed-wireless or narrowband IF path.

Selected Public Architecture & Frequency Sources

1. Broadcom BCM56980 Data Sheet—switch capacity, IEEE 1588 / SyncE support and core, TimeSync, BroadSync, PCIe and SerDes reference-clock requirements.
2. Cisco NCS 540 Medium Density Router Data Sheet—interfaces, SyncE / PTP timing roles, GNSS and model-dependent timing I/O.
3. Cisco NCS 540 External Timing Source Guide—1PPS, 10 MHz, ToD and BITS interface behavior.
4. Altera Agilex 7 E-Tile 10GE / 25GE PCS-only, OTN or FlexE Design Example—322.265625 MHz reference-clock example.
5. Microchip ZL30721 Product Brief—19.44 / 25 MHz input, 25 / 125 / 156.25 MHz output and TCXO / OCXO timing-card examples.
6. Microchip DS3106 Data Sheet and ZL30145 Data Sheet—telecom, SDH / SONET, Ethernet and OTN timing-frequency references.

Platform reference notice: Third-party platform names and published specifications are included for architecture reference only. Their inclusion does not imply adoption, approval, compatibility, endorsement or pin-to-pin replacement.

FCom APPLICATION ENGINEERING

Turn Your Clock Tree into a Qualified BOM

Share the system node, target IC, frequency, output logic, jitter/phase-noise target, stability/holdover requirement, temperature range and program quantities. FCom application engineering will recommend the appropriate series and confirm the configuration for quotation and sample validation.

Product parameters in this guide represent performance ranges from the current FCom portfolio. Final specifications and ordering codes are confirmed through FCom application review, quotation and approved product documentation.

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