

BROADBAND ACCESS TIMING

Broadband & Access Networks

Frequency-control solutions for fixed broadband, fiber access, cable access and selected fixed-wireless access equipment—supporting PHY clocking, high-speed SerDes references, network synchronization, clock recovery, local processing and architecture-dependent RF filtering.

Stable Access Timing + Cost-Effective Local Clocking + Low-Jitter SerDes References + Precision Synchronization

GPON / XG-PON / XGS-PON

OLT

ONU / ONT

Broadband Gateway

Remote PHY

Fixed Wireless Access

Engineering Focus

Identify the actual external clock node first—crystal input, CMOS clock input, differential SerDes REFCLK, DPLL / synchronization reference, RTC or RF reference—then select the FCom family that matches that node.

Architecture Consideration

System-level clock frequencies should be interpreted together with the selected SoC, PHY and timing architecture. For example, 125 MHz may be derived from a 25 MHz reference, while 122.88 MHz or 156.25 MHz may be generated within the clock tree.

25 MHz

Common external Ethernet PHY / local reference example.

122.88 MHz

Representative FWA baseband clock domain.

156.25 MHz

Representative 10GbE / XFI / SerDes REFCLK domain.

50 fs

FCO-2L/3L/5L-UJ jitter.

01

Application Scope & System Architecture

Broadband & Access Networks covers central-office fiber access, customer-premises gateways, distributed cable access and fixed-wireless access. Device selection follows the actual clock node—not the equipment name alone.

Fiber Access

- GPON / XG-PON / XGS-PON
- OLT / PON line cards
- ONU / ONT

Broadband CPE

- Residential / fiber gateways
- Multi-Gig Ethernet
- Wi-Fi / connectivity subsystems

Cable / DAA

- Remote PHY / RPD
- 10GbE backhaul
- RF ADC / DAC domains

Fixed Wireless Access

- Baseband / Ethernet / SerDes
- Precision local timing
- RF transceiver / front end

Clock Domains That Matter

Synchronization

PTP / SyncE / DPLL / holdover at infrastructure nodes

High-Speed REFCLK

10GbE / XFI / KR / SerDes reference

PHY / SoC Local Clock

Crystal or CMOS reference

RTC / Housekeeping

32.768 kHz low-power timing

RF Domain

FWA reference clock and band filtering where required

Crystal

Best fit when the PHY / SoC includes the oscillator circuit.

XO / Differential XO

Best fit when the IC requires a driven local or high-speed reference.

TCXO / VCXO / OCXO

Introduce only when accuracy, pullability, synchronization or holdover requires it.

SAW Filter

Use only in a real RF path with a defined band plan and rejection requirement.

Application note: SAW and MCF products apply only to specific RF or narrowband IF architectures. Mobile fronthaul and backhaul are covered separately under Switching, Routing & Mobile Transport.

02

Select by System Node First

The FCom series shown below are included where they provide a practical starting point for component selection. For other clock domains, confirm the receiving IC and external-clock topology before selecting a device.

System Node	Clock Function	Representative Frequency	Recommended FCom Series	Selection Considerations
ONU / ONT PHY	External crystal / local reference	25 MHz common example	FCX-2S / FCX-2M / FCX-3M	Package choice is useful only after CL / ESR and crystal-input requirements are confirmed.
Gateway RTC	RTC / sleep / housekeeping	32.768 kHz	FCT-1M / FCT-2M or FCO-6K-UC	Choose crystal vs driven XO from the RTC input topology; current and startup become key for low-power CPE.
10GbE / SerDes REFCLK	External high-speed differential reference	125 / 156.25 MHz class	FCO-2L-UJ / FCO-3L-UJ / FCO-5L-UJ	This family directly covers 100–220 MHz with differential output options and 50 fs jitter, making package, logic and supply selection the next key decisions.
Low-Power Gateway Clock	Local CMOS reference	≤50 MHz	FCO-2C-UP / FCO-3C-UP	Use when the system genuinely benefits from 0.9 / 1.2 / 1.5 V and low operating current.
Precision Access Timing	DPLL / synchronization reference	Timing-IC dependent	FVT-7S-WT for high-stability local timing; consider OCXO where holdover requirements justify it	Start from the required stability, aging, phase-noise, warm-up and holdover targets to determine whether TCXO or OCXO performance is appropriate.
FWA RF Reference	Wireless local reference	38.4 / 40 MHz class, chipset-dependent	FVT-6S / FVT-2S / FVT-3S	TCXO is useful only when the radio accuracy budget requires temperature compensation.

Match Performance to the Node

For cost- and power-sensitive ONU / gateway local clocks, a crystal or standard XO is typically the appropriate starting point; higher-stability devices are introduced only when the clock budget requires them.

Confirm the External Reference

A 125 MHz interface clock may be generated internally from a 25 MHz reference. Confirm the physical clock input before selecting the external frequency-control component.

Apply Performance Where It Adds Value

Low-jitter oscillators, precision TCXOs and OCXOs provide the greatest value at clock nodes with defined jitter, stability, synchronization or holdover requirements.

03

Frequency & Component Placement Matrix

Specific FCom series appear only where frequency directly helps narrow the choice. Elsewhere the table keeps the recommendation at device-class level.

Frequency	Typical Position	Architecture Status	FCom Direction	Engineering Interpretation
32.768 kHz	RTC / sleep / housekeeping	External local timing	FCT-1M / FCT-2M crystal; FCO-6K-UC driven XO	Crystal versus XO is a real topology choice; current, CL and startup matter.
25 MHz	Ethernet PHY / management PHY	Common external example	FCX-2S / FCX-2M / FCX-3M	Strong passive-reference opportunity; confirm CL and ESR.
38.4 / 40 MHz	Wi-Fi / modem / RF local reference	Chipset-dependent	Crystal or TCXO depending required frequency accuracy	Select a TCXO when the chipset and frequency-stability budget require temperature compensation; otherwise a crystal or standard XO may be sufficient.
100 MHz	Processor / FPGA / FWA clock tree	Platform example	CMOS or differential XO as required	Often a generated system clock; verify whether a discrete external source exists.
122.88 MHz	FWA baseband / telecom DSP	Platform example	Low-jitter XO / VCXO only if this is an external input	Public platform frequency does not prove a standalone oscillator.
125 MHz	GbE / SYSCLK	Often derived	XO only when the receiving IC exposes an external 125 MHz input	Frequently generated from 25 MHz; avoid premature part mapping.
156.25 MHz	10GbE / XFI / KR / SerDes REFCLK	High-value external class	FCO-2L-UJ / FCO-3L-UJ / FCO-5L-UJ	A strong fit for confirmed external high-speed references: 100–220 MHz coverage, differential outputs and 50 fs jitter.
RF band dependent	Selected FWA RF front end	Architecture-specific	FSF SAW filter selected only after RF requirements are known	Frequency alone is insufficient; Fc, BW, IL, rejection and impedance must be specified.

Selection note: map an FCom product to a platform frequency only after confirming that the frequency is required at a discrete external component position.

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Representative Platform & Architecture Matrix

The public platforms below illustrate representative access-network clock architectures. Product series are intentionally kept separate from the platform examples so that each clock domain can be evaluated on its own engineering requirements.

BROADCOM · FIBER ACCESS INFRASTRUCTURE

BCM68620 · Universal PON OLT

1

Public platform overview. Multi-protocol OLT SoC supporting GPON, XG-PON, XGS-PON, NG-PON2, EPON and 10G-EPON with burst-mode PON SerDes and high-speed NNI interfaces including 10G XFI.

Architecture insight. PON timing, high-speed NNI and network synchronization are separate clock domains.

Timing REF → OLT SoC → PON + 10G NNI

Engineering takeaway: synchronization, high-speed SerDes and local processor clock domains should be specified independently.

Source: broadcom.com/products/broadband/xpon/bcm68620

BROADCOM · FIBER CPE / GATEWAY

BCM68565 · 10G xPON Fiber Gateway

2

Public platform overview. Integrates PON MAC, 10GbE PHY, XFI/USXGMII-S, multiple 1GbE PHYs and local processing interfaces.

Architecture insight. Integration reduces discrete component count, making the remaining external references highly topology-dependent.

Local REF → Gateway SoC → PON + 10GbE / GbE

Engineering takeaway: confirm whether each interface requires a crystal, a driven reference clock, or relies on an internally generated clock.

Source: broadcom.com/products/broadband/xpon/bcm68565

BROADCOM · CABLE / DISTRIBUTED ACCESS

BCM31633 · DOCSIS 3.1 Remote PHY

3

Public platform overview. Combines RF ADC/DAC functions, DOCSIS processing, 10GbE connectivity and documented network-dejitter handling.

Architecture insight. Packet timing, SerDes reference and RF converter timing coexist but have different performance priorities.

Head-End Timing → 10GbE / RPD Local Clock → RF

Engineering takeaway: specify packet timing, SerDes reference and RF converter clock requirements independently.

Source: broadcom.com/products/broadband/cable/ccap-cmts/docsis-3-1-phy/bcm31633

NXP · FIXED WIRELESS ACCESS

LA1224-RDB · 5G FWA CPE Reference Design

4

Public platform overview. Public board information lists 122.88 / 156.25 / 125 MHz from one clock generator and 100 / 125 MHz from another, with IEEE 1588, GPS, SYSCLK, SerDes and Ethernet clock domains.

Architecture insight. The published frequencies are clock-tree outputs and should not be interpreted as requiring a separate oscillator for each frequency.

Precision REF → Clock Generator → Baseband + SerDes + Ethernet

Engineering takeaway: identify the upstream external reference and the actual IC clock inputs before selecting the frequency-control device.

Source: nxp.com/design/design-center/development-boards-and-designs/LA1224-RDB

05

Reference Design · Where Device Classes Belong

This page uses device classes to show the clock hierarchy before narrowing the selection to a specific FCom series.

REFERENCE DESIGN A

XGS-PON OLT → ONU/ONT → Gateway

OLT Timing / DPLL

PTP / SyncE / holdover

Precision TCXO / OCXO · Only when the synchronization and holdover budget requires it.

OLT NNI / SerDes

10GbE / XFI external REFCLK

Ultra-low-jitter differential XO · Use only for a confirmed external differential clock input.

ONU / ONT PHY

25 MHz-class external local reference

Quartz crystal / CMOS XO · Choose from the PHY input type and CL / ESR requirements.

Gateway Local Clock

Processor / connectivity

Standard or low-power CMOS XO · Power rail and current become relevant in compact CPE.

Gateway RTC

32.768 kHz

Tuning-fork crystal / ultra-low-current XO · Select according to the RTC input topology.

REFERENCE DESIGN B

Fixed Wireless Access CPE

Precision Local Reference

Timing IC / clock-generator input

High-stability TCXO · Use when the FWA timing architecture requires a precision upstream reference.

Baseband / Telecom Clock

122.88 MHz-class domain

Low-jitter XO / VCXO · Only if 122.88 MHz is an external input rather than a generated output.

Ethernet / SerDes

125 / 156.25 MHz-class

Differential XO · Logic and jitter requirements come from the receiving PHY / SerDes.

System Clock

100 MHz-class

CMOS XO · Only where the processor / FPGA exposes a discrete clock input.

RF Reference / Front End

Chipset and band dependent

TCXO + SAW filter · Selected independently from RF accuracy and band-selection requirements.

06

Choose the Device Class Before the Series

This page narrows the device architecture. Product series are introduced only in the next page, after the engineering decision is clear.

MHz Crystal

Use when: the PHY / SoC includes its own oscillator circuit.

Check frequency, CL, ESR, drive level, package and temperature.

32.768 kHz Crystal / XO

Use when: RTC / sleep / housekeeping timing is required.

Topology decides crystal vs driven clock; current and startup can dominate.

CMOS XO

Use when: the local clock input requires a driven single-ended reference.

Check supply, logic level, ppm, startup and power.

Differential XO

Use when: high-speed PHY / SerDes requires an external differential REFCLK.

Check LVDS/LVPECL/HCSL, jitter integration bandwidth and termination.

VCXO

Use when: a DPLL / clock-recovery loop explicitly requires pullability.

Pull range and control voltage matter more than nominal frequency alone.

TCXO

Use when: standard XO stability is insufficient.

Typical access use: precision local reference or wireless RF reference.

OCXO

Use when: infrastructure holdover / long-term stability justifies size and power.

Reserve OCXO for OLT or access-timing nodes that require its holdover and long-term stability performance.

SAW Filter

Use when: a selected FWA RF path needs band selection or interference suppression.

Filter selection starts from Fc, BW, IL, rejection and impedance—not from the application name.

07

Recommended FCom Product Families

The following FCom families are highlighted because they address the most common and technically distinct selection points in Broadband & Access Networks.

Selection Need	FCom Series	Key Specifications	Application Fit
25 / 40 MHz passive PHY / SoC reference	FCX-2S / FCX-2M / FCX-3M	2016 / 2520 / 3225 · ranges cover 25/40 MHz · ± 5 ppm tolerance · ± 10 ppm stability · $-40\sim+125^{\circ}\text{C}$	Lets the engineer choose package after CL / ESR requirements are known.
32.768 kHz RTC	FCT-1M / FCT-2M FCO-6K-UC if a driven clock is required	FCT: 1610 / 2012, $-40\sim+125^{\circ}\text{C}$. FCO-6K-UC: 1.5/1.8 V CMOS, ± 20 ppm, 1.4–1.8 μA , $-40\sim+105^{\circ}\text{C}$	Separates passive RTC crystal from ultra-low-current oscillator topology.
Low-voltage, low-power local clock	FCO-2C-UP / FCO-3C-UP	1–50 MHz · 0.9 / 1.2 / 1.5 V CMOS · 0.9–3 mA · ± 25 ppm · $-40\sim+85^{\circ}\text{C}$	Useful for compact ONU / gateway rails where a standard 1.8/2.5/3.3 V XO is not optimal.
125 / 156.25 MHz-class differential REFCLK	FCO-2L-UJ / FCO-3L-UJ / FCO-5L-UJ	100–220 MHz · LVPECL / LVDS / HCSL · ± 20 ppm · $-40\sim+125^{\circ}\text{C}$ · 50 fs jitter	Recommended for OLT NNI, Remote PHY and FWA SerDes nodes where a discrete high-speed differential REFCLK is required.
Precision access / FWA local reference	FVT-7S-WT	10–52 MHz · ± 50 ppb · $-40\sim+105^{\circ}\text{C}$ · phase noise to -156 dBc/Hz @10 kHz	Suitable for high-stability access and FWA reference nodes where TCXO performance meets the timing budget.
Infrastructure holdover / very-low-phase-noise reference	FOC-5S-LN	10–40 MHz · ± 5 ppb · $-40\sim+85^{\circ}\text{C}$ · -120 @10 Hz / -145 @100 Hz / -157 @1 kHz / -162 dBc/Hz @10 kHz	Use only if the timing architecture has a real holdover / phase-noise requirement that justifies OCXO size, power and warm-up.

FWA RF Filtering

For FWA RF filtering, select the **FSF SAW Filter** family after the target center frequency, bandwidth, insertion loss and rejection requirements are defined.

Frequency-Specific Ordering Code

The FCom product matrix primarily identifies oscillator and crystal **series**. Frequency-specific ordering codes are confirmed during technical review once the electrical and mechanical configuration is defined.

08

Engineering Validation & Minimum RFQ Inputs

A complete RFQ should identify the external component position before asking FCom to confirm a series or frequency-specific ordering code.

1 • Platform & Clock Node

- OLT / ONU / ONT / Gateway / RPD / FWA
- PHY / SoC / SerDes / DPLL / RTC / RF position
- External reference or internally generated clock?

2 • Electrical Interface

- Exact external frequency
- Crystal or driven clock
- CMOS / LVDS / LVPECL / HCSL / clipped sine
- Supply and enable / standby function

3 • Crystal Inputs

- Load capacitance (CL)
- Maximum ESR
- Drive level / gain margin if specified

4 • Jitter / Phase Noise

- RMS jitter limit and integration bandwidth
- Receiver / SerDes reference-clock mask
- RF synthesizer phase-noise requirement

5 • Stability / Timing

- Temperature stability and aging
- PTP / SyncE / DPLL architecture
- Holdover target and OCXO power / warm-up budget

6 • RF / Commercial

- SAW Fc / BW / IL / rejection / impedance
- Package / operating temperature
- Prototype quantity, sample date and annual volume

Send the clock node, exact external frequency, electrical interface, stability / jitter requirement, temperature and package.
Request Technical Review →

09

Engineering FAQ & Application Review

Is 125 MHz always a discrete oscillator?

No. It is a common GbE system/interface clock, but many PHYs derive it from a lower external reference such as 25 MHz.

When should I consider the FCO-xL-UJ family?

Consider the FCO-xL-UJ family when the design requires an external 100–220 MHz differential reference. Its 50 fs jitter, output-logic options and package choices are then directly relevant to the selection.

Does an ONU / ONT need a TCXO?

Not by default. Start from the chipset's crystal or driven-clock input. TCXO is justified only when the required frequency accuracy exceeds standard local-clock capability.

When is OCXO appropriate?

At selected infrastructure timing nodes where holdover, aging or phase noise creates enough value to justify additional size, power and warm-up.

Are 122.88 / 156.25 MHz platform frequencies always standalone XOs?

No. They may be outputs of a clock generator. The external reference architecture must be checked before selecting a discrete oscillator.

Why are exact SAW filter P/Ns omitted from the main guide?

Because FWA filter selection is band-plan-specific. A general application PDF should route the customer to an RF review rather than imply that one published filter fits every FWA design.

Primary Public Architecture References

1. **Broadcom BCM68620** — universal OLT PON MAC and high-speed NNI architecture: Broadcom BCM68620
2. **Broadcom BCM68565** — integrated 10G xPON gateway SoC: Broadcom BCM68565
3. **Broadcom BCM31633** — DOCSIS 3.1 Remote PHY with 10GbE and RF converter domains: Broadcom BCM31633
4. **NXP LA1224-RDB** — public FWA multi-domain clock-tree example: NXP LA1224-RDB

Need a Broadband Timing Recommendation?

Send the actual clock node and electrical requirement. FCom engineering can confirm whether the right answer is a crystal, XO, low-jitter differential clock, TCXO, VCXO, OCXO or RF filter—and then provide the frequency-specific order code.

[General Inquiry](#)
[Technical Support](#)

Product-data basis: FCom in-sale product matrix supplied 18 Aug 2026. Product families are presented where they provide direct selection value. Final device selection and the frequency-specific ordering code are confirmed during engineering review.