

BATTERY & POWER CONVERSION

BMS, Charging & Power Electronics

Reliable controller, communication and standby timing for battery-management, charging and power-electronics systems operating near switching noise and across wide temperature ranges.

Controller Timing + Communication Timing + Standby Timing + Wide Temperature + Switching-Noise Robustness

Battery Management Systems

On-Board Chargers

DC Fast Charging

DC/DC Converters

Inverters / PCS

Energy Storage

Application Scope

Battery and power-conversion platforms combining real-time control, precision measurement, vehicle / industrial communications, standby timekeeping and high-energy switching stages.

Selection Philosophy

Select by system node first. External crystals and oscillators normally sit at the MCU, DSP, FPGA, PHY or standby domain. PWM, ADC sample and power-switching frequencies are generally derived clocks.

Control

BMS MCU, safety MCU, digital-power MCU / DSP and FPGA reference timing.

Communication

CAN / CAN FD, Ethernet PHY, RMII and gateway clocking.

Standby

RTC, sleep / wake scheduling, event logging and low-power supervisory timing.

Environment

Wide temperature, startup margin, EMI and routing near high-dv/dt / high-di/dt nodes.

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Application Scope & Engineering Domains

Separate the control, communication, standby and power-stage domains before assigning any external timing component.

BMS, Charging & Power Electronics combines sensitive low-voltage timing circuitry with high-current switching, isolation and wide thermal variation. The correct timing device is selected from the controller or interface clock architecture—not from the converter's nominal power level or switching frequency.

Typical Equipment

Battery Management

Battery Management Unit (BMU)
Cell Monitoring Unit (CMU)
Battery Junction / Disconnect Unit
Safety Controller / Gateway

Charging Systems

On-Board Charger (OBC)
AC Charger Controller
DC Fast Charger Power Module
Charging Communication Controller

Power Electronics

PFC / AFE
DC/DC Converter
Inverter / PCS
ESS Power Conversion

Four Engineering Domains

Controller Timing

MCU / DSP / FPGA external reference and the PLL / system-clock tree derived from it.

Communication Timing

CAN / CAN FD host timing, Ethernet PHY clocks, RMII references and gateway interfaces.

Standby Timing

32.768 kHz RTC, wake scheduling, backup timing and event-log time base.

Power-Stage Environment

High dv/dt, high di/dt, ground noise, local thermal rise and EMI susceptibility.

Main Technical Requirements

Startup Margin

ESR · CL · drive level · negative resistance · startup across temperature.

Frequency Accuracy

Initial tolerance · temperature stability · aging · system ppm budget.

Clock Interface

Crystal vs CLKIN · CMOS / differential logic · duty cycle · OE / standby.

Environmental Fit

AEC requirement · local PCB temperature · noise coupling · routing constraints.

Application boundary: cell-monitor AFEs, gate drivers and SiC / GaN / IGBT power devices typically use internal or controller-derived timing. An external crystal or oscillator should be selected only where the target IC provides a documented external timing interface.

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Select by System Node First

Begin with the actual external clock node, then choose crystal / XO architecture, frequency, qualification and package.

Representative FCom series are shown only where they resolve a real selection branch. The final configuration remains dependent on the target MCU / DSP / PHY and board-level clock circuit.

System Node	Typical Function	Representative Reference	Typical Device	Selection Focus
RTC / Standby / Wake	Low-power time base	32.768 kHz	Tuning-fork crystal / kHz XO	RTC topology, CL, ESR, standby current, backup supply
BMS / Safety MCU	Main controller reference	8–40 MHz class	MHz crystal / CMOS XO	XTAL vs CLKIN, startup margin, AEC requirement, temperature
Digital-Power MCU / DSP	Source for ADC / PWM / control loop	16 / 20 / 24 / 25 MHz class	Crystal / CMOS XO	Controller clock tree, PLL range, local thermal zone
Ethernet PHY	PHY reference	25 MHz	Crystal / XO	Crystal-input vs driven-clock mode, ppm budget, CL
RMII / MAC-PHY	Externally driven interface clock	50 MHz	CMOS XO	REF_CLK direction, logic level, duty cycle, source/load topology
Gateway / FPGA / High-Speed Network	Logic / Ethernet / high-speed reference	100 / 125 / 156.25 MHz	Low-jitter CMOS / differential XO	RMS jitter, LVDS / LVPECL / HCSL, termination, signal integrity
Gate Driver / Power Stage	PWM sink / switching element	Controller-derived	Typically controller-derived timing	Evaluate dead time, isolation delay and switching behavior at the controller / driver level

Automotive Crystal Path

When the controller exposes XTAL pins and AEC-Q200 is required, begin with the **FCX-A family**. Select the package only after frequency, CL / ESR and oscillator-margin checks.

Driven-Clock Path

When the IC requires CLKIN or a complete CMOS oscillator is preferred, **FCO-6C** is a representative compact option up to 50 MHz. Wider-temperature alternatives can be evaluated where the system thermal requirement calls for them.

Standby Path

Where an external 32.768 kHz crystal is explicitly required, **FCT-3M-A** is a representative AEC-Q200 option. If the RTC already integrates its timing element, no additional external 32.768 kHz crystal is normally required.

Recommended selection sequence: System node → external vs derived → crystal vs driven clock → frequency → qualification / temperature → package → FCom series → final electrical configuration.

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Frequency & Component Placement Matrix

Use representative external references together with system position and clock topology. Internal CPU, PWM and ADC rates are intentionally excluded.

System Position	Typical Frequency	Primary Function	Reference / Applicability	Preferred Device
RTC / Standby	32.768 kHz	Timekeeping / wake / event log	Common External Reference	Crystal / low-power XO
BMS MCU	8 / 16 / 24 / 40 MHz class	Main controller reference	Common External Reference	MHz crystal / CMOS XO
Digital-Power MCU / DSP	16 / 20 / 24 / 25 MHz class	PFC / DC-DC / inverter controller reference	Common External Reference	Crystal / CMOS XO
Ethernet PHY	25 MHz	PHY reference clock	Common External Reference	Crystal / XO
RMII / MAC-PHY	50 MHz	External REF_CLK	Interface-Dependent	CMOS XO / driven clock
Gateway / FPGA	100 / 125 / 156.25 MHz	Logic / network reference	Architecture-Dependent	Low-jitter XO / differential XO
MCU CPU Clock	80 / 120 / 160 MHz+	Internal processing domain	Usually Internally Derived	Verify whether an external reference is actually required
PWM / Switching	kHz to MHz switching range	Gate-drive timing	Derived from Controller	Derived timing; select the external reference at the controller node
ADC Sampling	Controller / ADC dependent	Measurement timing	Derived / Peripheral Clock	Validate controller clock tree

Automotive Qualification

For an external-crystal controller node requiring AEC-Q200 and –40 to +125°C operation, the **FCX-A** family provides the relevant FCom selection range.

Driven CMOS Clock

For a CMOS CLKIN architecture up to 50 MHz, **FCO-6C** is a representative compact option. Wider-temperature families can be evaluated where the operating environment requires additional margin.

High-Speed Low-Jitter Clocking

For 100–220 MHz differential nodes with an explicit low-jitter requirement, **FCO-2L-UJ** is a representative option. This performance class is generally intended for gateway, FPGA and high-speed network domains rather than standard BMS / OBC controller clocks.

50 MHz note: Ethernet clocking is architecture-dependent. Many PHYs use a 25 MHz crystal, while selected RMII architectures require a driven 50 MHz reference.

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Representative Platform & Architecture Examples

Public reference platforms illustrate where controller, communication and standby clock domains appear in real BMS and power-conversion systems. FCom series should be selected independently against the electrical and environmental requirements of the final design.

NXP

RD-K358BMU · 800 V HVBMS

1

Architecture: S32K358-based Battery Management Unit within an 800 V HVBMS architecture, with CAN/CAN FD, BMS communication and RTC / wake functions.

Clock evidence: S32K3 supports an 8–40 MHz FXOSC and a 32.768 kHz SXOSC. The specific BMU includes PCA2131 RTC; therefore the standby-clock implementation should be confirmed at platform level before specifying an external 32.768 kHz crystal.

Cell / Pack Sensing → BMU Controller → CAN / Gateway / RTC

Selection insight: treat the BMU controller, network interface and standby domain as separate clock decisions.

TEXAS INSTRUMENTS

PMP22650 · 6.6 kW Bidirectional OBC

2

Architecture: two-phase totem-pole PFC + full-bridge CLLC, controlled by a TMS320F28388D real-time controller.

Clock evidence: public F28388D controlCARD designs document 20 MHz and 25 MHz external reference-clock implementations; the converter's 120 kHz / 200–800 kHz switching rates are derived.

20 / 25 MHz Ref. → Real-Time MCU → ADC / PWM / Control

Selection insight: keep the external controller reference separate from the switching-frequency discussion.

INFINEON

REF-EV50KW2SICKIT · 50 kW DC Charger

3

Architecture: 3-phase active front end + 3-phase DAB; the power-control board uses AURIX TC377 for ADC, diagnostics, CAN and PWM generation.

Clock evidence: the public guide identifies controller and topology but does not publish the fitted controller-board crystal frequency.

Voltage / Current Sense → AURIX Control → PWM → SiC Stage

Selection insight: confirm the exact controller oscillator circuit and local thermal zone before defining the external reference frequency.

STMICROELECTRONICS

STEVAL-7BIDIRCB · 7 kW Bidirectional AC/DC

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Architecture: interleaved totem-pole PFC + bidirectional CLLC, digitally controlled by two STM32G474 MCUs on one control card.

Clock evidence: STM32G474 supports a 4–48 MHz external crystal oscillator and a 32 kHz oscillator; the platform page does not state the fitted HSE frequency.

Controller #1 → PFC + DC Link → Controller #2 / CLLC

Selection insight: multi-controller systems can contain multiple independent reference-clock decisions.

Platform interpretation: these examples are provided for architecture reference. FCom component selection is independent of the cited platforms and should be verified against the exact IC documentation, customer schematic and complete system requirements.

05

800 V HVBMS Timing Architecture

Representative placement of external timing from cell / pack sensing through the BMU controller to standby and network domains.

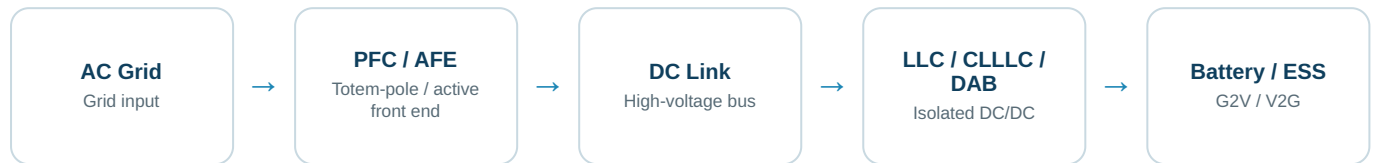
LAYER 1 Cell & Pack Sensing	Cell Monitor / AFE Voltage, temperature, balancing and pack measurement functions.	Timing Role Often internal or communication-derived.	External Timing Requirement An external quartz device is relevant only where the selected AFE provides a documented oscillator or clock input.
LAYER 2 BMU / Safety MCU	SOC / SOH · Diagnostics · Contactors Main safety and battery-control processing domain.	8–40 MHz class Representative external MCU reference range.	FCX-A Family Applicable where the MCU exposes XTAL pins and AEC-Q200 is required. FCX-3M-A provides broad 3225 coverage from 8–50 MHz; smaller packages can be evaluated after confirming frequency, CL / ESR and oscillator margin.
LAYER 3 Standby / RTC	Sleep · Wake · Event Logging Low-power timekeeping and supervisory domain.	32.768 kHz Applicable where the standby / RTC domain provides an external low-speed crystal node.	FCT-3M-A AEC-Q200 32.768 kHz crystal, 3215 package, –40 to +125°C. Where the RTC already integrates its timing element, an additional external crystal is normally unnecessary.
LAYER 4 Vehicle / System Network	CAN FD · Ethernet · Gateway Vehicle-network communication and external system interface.	25 / 50 MHz 25 MHz PHY crystal/XO; 50 MHz driven RMII where required.	Choose by PHY Mode Use a crystal only for a crystal-input PHY; use a CMOS XO where the interface requires driven REF_CLK.
Crystal Priority CL, ESR, drive level and negative-resistance margin must be checked against the selected MCU oscillator circuit.			
Qualification Priority AEC qualification is a separate requirement from temperature range; confirm both explicitly.			
Standby Priority Confirm whether the RTC or companion device already integrates its 32.768 kHz timing source before specifying an external crystal.			

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Bidirectional Charger / PCS Timing Architecture

Representative power-conversion architecture showing where the external controller clock sits relative to PFC, isolated DC/DC and high-energy switching stages.

Power Path



Controller Clock Path



Crystal-Input Controller

Use when the MCU/DSP includes a suitable oscillator circuit and passive crystal routing is appropriate.

Representative FCom options: FCX-2S-A / FCX-2M-A

Driven CMOS Clock

Use when CLKIN is specified or an active source gives a clear board-level advantage.

Representative FCom option: FCO-6C

Wider Thermal Envelope

A wider-temperature oscillator can be evaluated where local system conditions require additional thermal margin.

Representative option: FCO-2C-WT

Switching-noise design: keep the crystal loop short; separate clock routing from high-dv/dt switch nodes and gate-drive paths; maintain clean return paths; verify startup, ESR and drive level while the converter is operating across temperature.

Derived-frequency rule: 48 kHz, 100 / 120 kHz, 200–800 kHz and similar converter switching rates are generated from the controller clock tree and therefore should be treated separately from the external crystal / oscillator reference.

07

FCom Selection Guidance by Design Condition

Representative FCom series are introduced where electrical, qualification, thermal or jitter requirements create a meaningful component-selection decision.

AEC-Q200 Crystal

For controller nodes where automotive qualification is explicit.

32.768 kHz Standby

For real external RTC / wake timing nodes only.

Driven CMOS Clock

For CLKIN / REF_CLK architectures requiring an active source.

Low-Jitter Extension

For FPGA / gateway / high-speed network nodes with explicit jitter limits.

Design Condition	Representative FCom Series	Key Catalog Specifications	When to Use
External crystal + AEC-Q200	FCX-A family FCX-3M-A / FCX-2S-A	FCX-3M-A: 3225 · 8–50 MHz · ±10 ppm tolerance · ±50 ppm stability · –40 to +125°C. FCX-2S-A: 2016 · 16–52 MHz · same qualification / temperature positioning.	BMS / safety MCU and charging-controller XTAL inputs where AEC-Q200 is required.
External 32.768 kHz standby crystal	FCT-3M-A	3215 · 32.768 kHz · ±10 ppm · –40 to +125°C · 6–12.5 pF · ESR 70 kΩ · AEC-Q200.	RTC / sleep / wake nodes where the receiving device provides an external tuning-fork oscillator circuit.
Driven CMOS clock up to 50 MHz	FCO-6C	2016 · 1.5–50 MHz · 1.8 / 2.5 / 3.3 V · ±20 ppm · –40 to +125°C · CMOS.	CLKIN / REF_CLK controller or PHY architecture where an active source is preferred.
Wider temperature / higher CMOS frequency	FCO-2C-WT	2520 · 1.25–100 MHz · 1.8 / 2.5 / 3.3 V · ±30 ppm · –55 to +125°C · CMOS.	Industrial charger / PCS nodes where the wider low-temperature envelope or frequency range is actually required.
High-speed differential + explicit low jitter	FCO-2L-UJ	2520 · 100–220 MHz · 1.8 / 2.5 / 3.3 V · LVPECL / LVDS / HCSL · –40 to +125°C · 50 fs listed RMS jitter.	Conditional gateway / FPGA / high-speed Ethernet nodes—not ordinary BMU / OBC control clocks.
Complete low-current 32.768 kHz clock	FCO-6K-UC	2016 · 32.768 kHz · 1.5 / 1.8 V · ±20 ppm · –40 to +105°C · 1.4–1.8 μA.	Standby domain requiring a driven 32.768 kHz output rather than a passive crystal; AEC qualification not stated in the supplied matrix.

Architecture-specific extensions: VCXO, OCXO, Crystal Filter, SAW Resonator and SAW Filter remain available within the wider FCom portfolio for designs that introduce tuning, ppb-class accuracy, RF or filtering requirements. TCXO is similarly considered where tighter temperature-compensated frequency accuracy is required beyond the standard crystal / XO path.

ENGINEERING SELECTION SUPPORT

Request an FCom Timing Recommendation

Send the target MCU / DSP / PHY and clock pin together with frequency, CL / ESR or supply / output, stability, temperature, qualification and package constraints.

[Start Engineering Review →](#)

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Engineering Validation & Selection Checklist

Confirm the oscillator circuit, electrical limits, local environment and project qualification before final component selection.

Quartz Crystal

- Frequency, CL, ESR, C0 and drive level
- Initial tolerance and temperature stability
- Negative resistance and startup margin
- Target MCU / PHY oscillator circuit
- AEC-Q200 requirement where applicable

CMOS / Differential XO

- Supply voltage and input logic
- Duty cycle, rise / fall and OE behavior
- Termination / fan-out / signal integrity
- Jitter integration bandwidth where specified
- Local thermal range and qualification requirement

Standby / 32.768 kHz

- Crystal oscillator vs driven clock input
- CL / ESR or output voltage requirement
- Backup-supply / standby-current budget
- Accuracy across temperature
- Verify whether an RTC already integrates its timing element

Power-Stage Environment

- Crystal-loop placement and routing
- Distance from gate-drive and switch nodes
- Ground / return-current integrity
- Local PCB temperature near magnetics and power devices
- Startup validation while the converter is actively switching

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	BMS / OBC / DC charger / inverter / PCS / DC-DC; identify BMU MCU, digital-power controller, PHY, RTC, FPGA or other clock node.
Target IC	Exact MCU / DSP / FPGA / PHY part number and the relevant XTAL / CLKIN / RTC / REF_CLK pin or schematic section.
Quartz Crystal	Frequency, package, CL, ESR, tolerance, temperature stability, drive level and AEC / reliability requirement.
XO / Differential XO	Frequency, supply, output logic, stability, temperature, jitter target, duty cycle, OE / standby and termination / load information.
Project / Program	Prototype quantity, required sample date, annual volume, qualification timing, production site and special environmental constraints.

Clock Architecture

Confirm external crystal vs driven clock before comparing part families.

Thermal Zone

Specify the timing-device PCB temperature, not only system ambient.

Frequency Classification

Mark each frequency as external reference, platform-dependent, derived or conditional.

Frequency alone is not sufficient: “20 MHz” still requires CL / ESR / temperature / qualification for a crystal or supply / output / stability for an XO. The final FCom ordering code follows the complete electrical specification.

09

Engineering FAQ & Application Review

Common interpretation questions, selection boundaries and representative public architecture references.

Is the converter PWM frequency a crystal frequency?

No. PWM and switching rates are normally derived from the MCU / DSP clock tree. Select the external crystal or XO from the controller's documented reference-clock requirement.

Should every BMS cell-monitor AFE have its own crystal?

No. Many AFEs use internal or communication-derived timing. The BMU / safety MCU, network and standby domains are more typical external-quartz locations.

Can 50 MHz be called an Ethernet crystal?

Not generically. Many PHYs use a 25 MHz crystal, while some RMII modes require a driven 50 MHz REF_CLK. Check the exact PHY / MAC architecture first.

When should a TCXO be considered?

Consider a TCXO when the required frequency accuracy over temperature exceeds the capability of the standard crystal / XO path. For most controller nodes, crystal or XO solutions remain the primary architecture.

Does -40 to +125°C automatically mean automotive qualified?

No. Temperature range and AEC qualification are separate attributes. AEC-Q200 is identified in this guide only for FCom families explicitly listed with that qualification in the supplied product matrix.

When does a low-jitter differential XO become relevant?

It becomes relevant for documented high-speed FPGA / gateway / Ethernet reference nodes with explicit jitter and output-logic requirements; standard controller clocks generally do not require this performance class.

Representative Public Technical References

1. **NXP:** RD-K358BMU — S32K358 Battery Management Unit for 800 V HVBMS.
2. **Texas Instruments:** PMP22650 — 6.6 kW bidirectional on-board charger reference design.
3. **Infineon:** REF-EV50KW2SICKIT — 50 kW DC EV charger reference design and user guide.
4. **STMicroelectronics:** STEVAL-7BIDIRCB — 7 kW bidirectional AC/DC converter for ESS / industrial charging.

FCom product specification note: product information in this guide is presented at the series or representative-configuration level. Exact ordering codes, guaranteed limits and availability should be confirmed against the applicable FCom datasheet and quotation.

ENGINEERING REVIEW

BMS, Charging & Power Electronics Timing Review

Share the target IC / module, exact clock node, external frequency, CL / ESR or supply / output, stability, temperature, package, qualification and project stage. FCom can review the requirement and recommend an appropriate product series and configuration.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection should be verified against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.