

AR/VR, SMART GLASSES & SPATIAL DEVICES

AR/VR, Smart Glasses & Spatial Devices

This guide helps designers coordinate compact mobile-class references, display and perception clocks, low-latency wireless timing, and high-speed interface references across immersive and spatial-computing devices.

XR Compute + Near-Eye Display + Camera / Sensor Fusion + Wireless + High-Speed Interfaces

VR Headsets

AR / Smart Glasses

Mixed Reality

Spatial Computing

Eye / Hand Tracking

Wireless Viewers

Application Scope

Integrated XR headsets, distributed smart-glasses architectures, display engines, tracking cameras, sensor hubs, audio subsystems, wireless links and PCIe / high-speed peripheral interfaces.

Selection Philosophy

Selection begins with the receiving clock node. Processor, display, camera, radio, audio, RTC and high-speed interfaces remain separate timing domains even when integrated into one wearable platform.

Compute

XR SoC, co-processor, ISP, DSP and sensor-hub references.

Display

Display controller, projection engine and panel timing.

Perception

Global-shutter cameras, eye tracking, SLAM and IMU timing.

Connectivity

Wi-Fi, Bluetooth, GNSS, audio and high-speed I/O.

01

Application Scope & Engineering Domains

Immersive devices combine mobile compute, display, perception and connectivity functions whose external timing requirements must be evaluated independently.

Integrated VR / MR Headset

A high-performance XR SoC manages dual displays, multiple cameras, sensor fusion, audio and local wireless connectivity.

Distributed Smart Glasses

An on-glass processor and co-processor handle latency-sensitive perception while selected workloads are transferred to a host over a low-latency wireless link.

Spatial Device / Compute Puck

Compute, networking and high-speed I/O may be separated from the display assembly, creating additional PCIe, USB, display and inter-board clock boundaries.

XR Compute

SoC, GPU, DSP, ISP and sensor-hub references are commonly multiplied internally from one or more external sources.

Near-Eye Display

Display controllers and projection engines may require a local crystal or driven clock independently of display-link timing.

Vision & Sensors

Camera XCLK, frame synchronization, strobe, IMU sampling and ISP capture belong to related but distinct timing layers.

Wireless & I/O

Wi-Fi / Bluetooth, GNSS, audio MCLK and PCIe REFCLK are selected by their own receiver interfaces.

Always-On

32.768 kHz RTC / wake timing



Compute / Radio

19.2 / 26 / 32 / 38.4 / 40 MHz class



Display / Camera

24 / 27 MHz; sensor-specific XCLK



Audio

12.288 / 24.576 / 49.152 MHz class



High-Speed I/O

25 MHz generator input or 100 MHz REFCLK

Reference Frequency

The external frequency is defined at the receiving XTAL or CLKIN node—not by CPU frequency, display refresh rate or interface line rate.

Clock Quality

Jitter and phase-noise limits matter only when tied to the receiver's integration band, clock topology and system latency budget.

Physical Integration

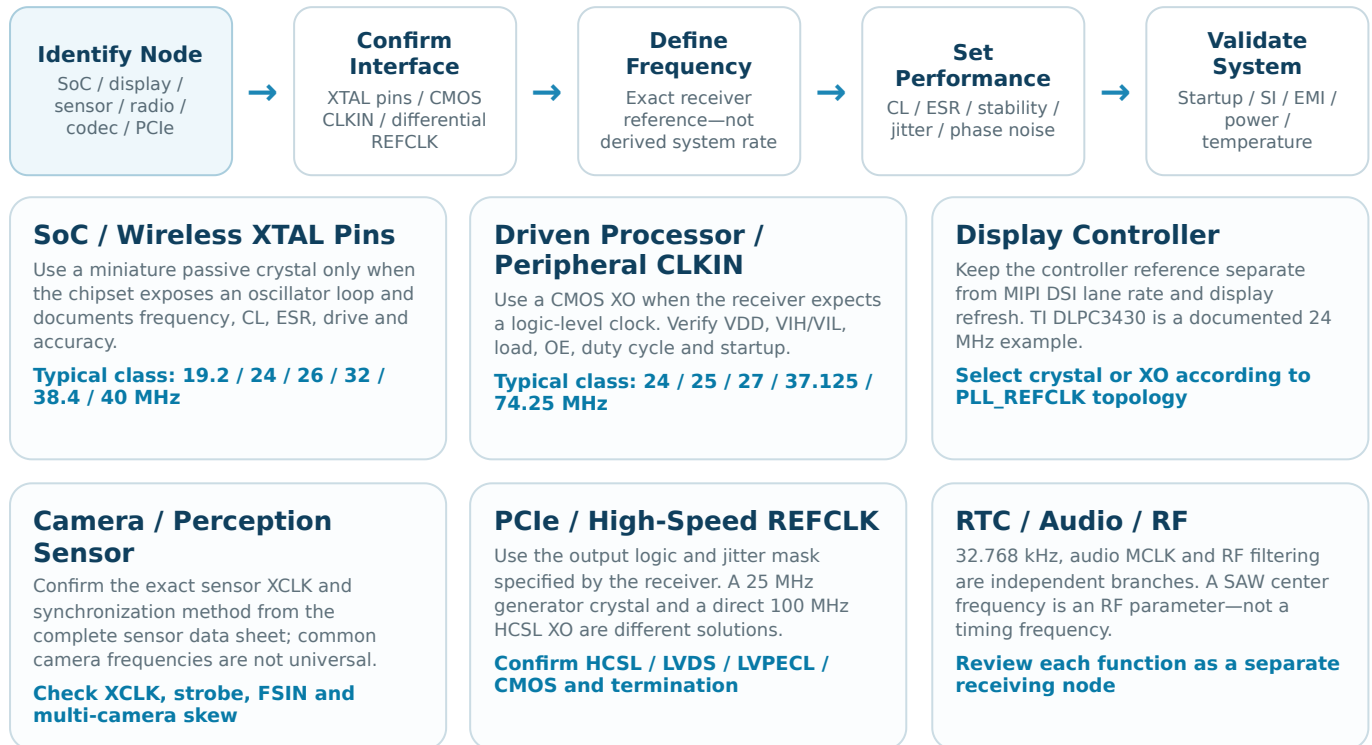
A SOM or radio module may integrate its crystal. An external host-board timing component is relevant only where a documented clock input is exposed.

System-rate boundary: 90 / 120 Hz display refresh, 120 fps camera operation, MIPI lane rate, Wi-Fi throughput and PCIe generation do not directly specify the external crystal or oscillator frequency.

02

Select by System Node First

Identify the receiving device and clock interface before selecting frequency, passive-crystal or driven-clock topology, output format and performance class.



Topology rule: a passive crystal and an active oscillator are not interchangeable merely because they share a nominal frequency. The receiving circuit determines the component class.

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Frequency & Component Placement Matrix

The frequency families below are practical architecture checkpoints. Final values remain controlled by the exact receiving device and schematic.

Frequency / Band	Representative System Node	Device Class	Selection Boundary
32.768 kHz	RTC, sleep timer, sensor hub, wake controller	Low-Power Timebase	Use a tuning-fork crystal for XTAL pins or a low-current XO only for a documented driven CLKIN.
12.288 / 24.576 / 49.152 MHz	Codec, DAC, ADC or DSP audio MCLK	Conditional Audio Clock	Select only where an exposed MCLK input and the required 48 kHz-family ratio are documented.
19.2 / 26 / 32 / 38.4 / 40 MHz	XR SoC, wireless IC, GNSS, sensor hub	Platform-Specific Reference	Do not infer the frequency from the platform name. Check whether the clock is chip-down, PMIC-generated or module-integrated.
24 / 27 MHz	Display controller, camera sensor, video bridge	Common Vision / Display	24 MHz is directly public for DLPC3430; camera values remain sensor-specific.
25 MHz	Clock generator, Ethernet PHY, system reference	Architecture-Dependent Input	May feed a generator that produces 100 MHz PCIe clocks; it is not equivalent to a direct 100 MHz source.
37.125 / 74.25 MHz	Selected image sensors and video paths	Conditional Sensor XCLK	Use only when the selected sensor data sheet explicitly requires the exact frequency.
100 / 125 / 156.25 MHz	PCIe, FPGA, bridge, SerDes and high-speed I/O	Low-Jitter REFCLK	Match output logic, swing, common mode, termination and the receiver's jitter integration band.
1176.45 / 1575.42 / 2442 MHz class	GNSS L5 / L1 and 2.4 GHz RF receive path	RF Filter — Not a Clock	Center frequency, bandwidth and insertion loss are RF parameters; use only at a defined filter position.

Always-On
32.768 kHz RTC / wake / retention domain.

Mobile Reference
19.2 / 26 / 32 / 38.4 / 40 MHz platform-specific domain.

Vision / Display
24 / 27 MHz and sensor-specific XCLK domain.

High-Speed
25 MHz generator input or 100 / 125 / 156.25 MHz REFCLK.

Frequency Match
Confirm that the selected FCom series covers the exact external frequency rather than a nearby video, radio or interface value.

Electrical Match
Passive CL / ESR and active VDD / output logic / load requirements must match the receiving circuit.

Performance Match
Wireless accuracy, camera synchronization, audio jitter and PCIe phase jitter are different specifications.

Interpretation: interface frequency, lane rate, frame rate and RF center frequency must not be relabeled as an oscillator requirement. Use the receiving clock pin as the source of truth.

04 Representative Platform & Architecture Matrix

Four public architectures illustrate distributed smart-glasses processing, integrated XR compute, near-eye display timing and global-shutter perception boundaries.

QUALCOMM

Snapdragon AR2 Gen 1 · Distributed Smart Glasses

1

Architecture: an AR processor, AR co-processor and FastConnect 7800 platform distribute latency-sensitive work within the glasses and exchange selected workloads with a phone or PC host.

Publicly documented features: support for up to nine concurrent cameras and sustained host-link latency below 2 ms; available public documentation does not disclose board-level crystal or XO values.

Host Device ↔ Wi-Fi 7 ↔ AR Co-Processor

Engineering interpretation: processor, co-processor, wireless and sensor references should be treated as separate schematic checkpoints. A mobile-reference frequency is assigned only after review of the applicable hardware design documentation.

THUNDERCOMM

TurboX C865C SOM · Integrated XR Compute

2

Architecture: the QCS8250-based SOM combines compute, ISP, wireless and storage while exposing dual MIPI DSI, multiple MIPI CSI, PCIe and USB interfaces for AR/VR platforms.

Publicly documented features: the module documents display, camera and high-speed interfaces, but not its internal board-level references.

Internal References → C865C SOM → DSI / CSI / PCIe

Engineering interpretation: timing sources integrated within the SOM remain inside the module boundary. Component selection applies only to documented carrier-board or peripheral clock inputs.

TEXAS INSTRUMENTS

DLP2010AFQJ + DLPC3430CZVBR · Near-Eye Display

3

Architecture: a DLP2010 DMD, DLPC3430 controller and DLPA200x / DLPA3000 power / LED device form a compact display engine.

Published clock requirements: DLPC3430 requires 24.000 MHz, 23.998–24.002 MHz, ±200 ppm total; the crystal recommendation is fundamental, CL 6 pF, ESR 120 Ω max. and 1 ms startup max.

24 MHz XTAL / XO → DLPC3430 → DLP2010 DMD

Engineering interpretation: this is a direct external-clock selection point. Pixel clock and MIPI lane rate remain separate interface parameters.

OMNIVISION

OG0VE · Global-Shutter Perception Camera

4

Architecture: OG0VE1B-A25A-001A / OG0VE1B-GA4A-001A target SLAM, gesture, head / eye tracking and depth / motion sensing.

Publicly documented features: VGA up to 120 fps, one-lane MIPI D-PHY up to 800 Mbps, two on-chip PLLs and built-in strobe; the public brief does not state external XCLK frequency.

Sensor XCLK* → OG0VE / PLLs → MIPI CSI / ISP

Engineering interpretation: confirm XCLK from the complete sensor data sheet before selecting a clock source. Frame rate and MIPI lane rate are not oscillator frequencies.

Platform-use boundary: third-party platforms are cited solely to illustrate architecture and clock-insertion boundaries. They do not imply FCom adoption, qualification, endorsement, verified compatibility or drop-in replacement.

Distributed AR

Host, connectivity and on-glass processing form separate domains.

Integrated SOM

Internal references remain inside the certified module boundary.

Display Engine

24 MHz is a public, directly selectable controller reference.

Perception Sensor

XCLK is selected only after the complete sensor specification is reviewed.

05

Integrated VR / MR Headset Timing Architecture

Representative timing from compact processor and display references through camera domains and low-jitter high-speed interfaces.

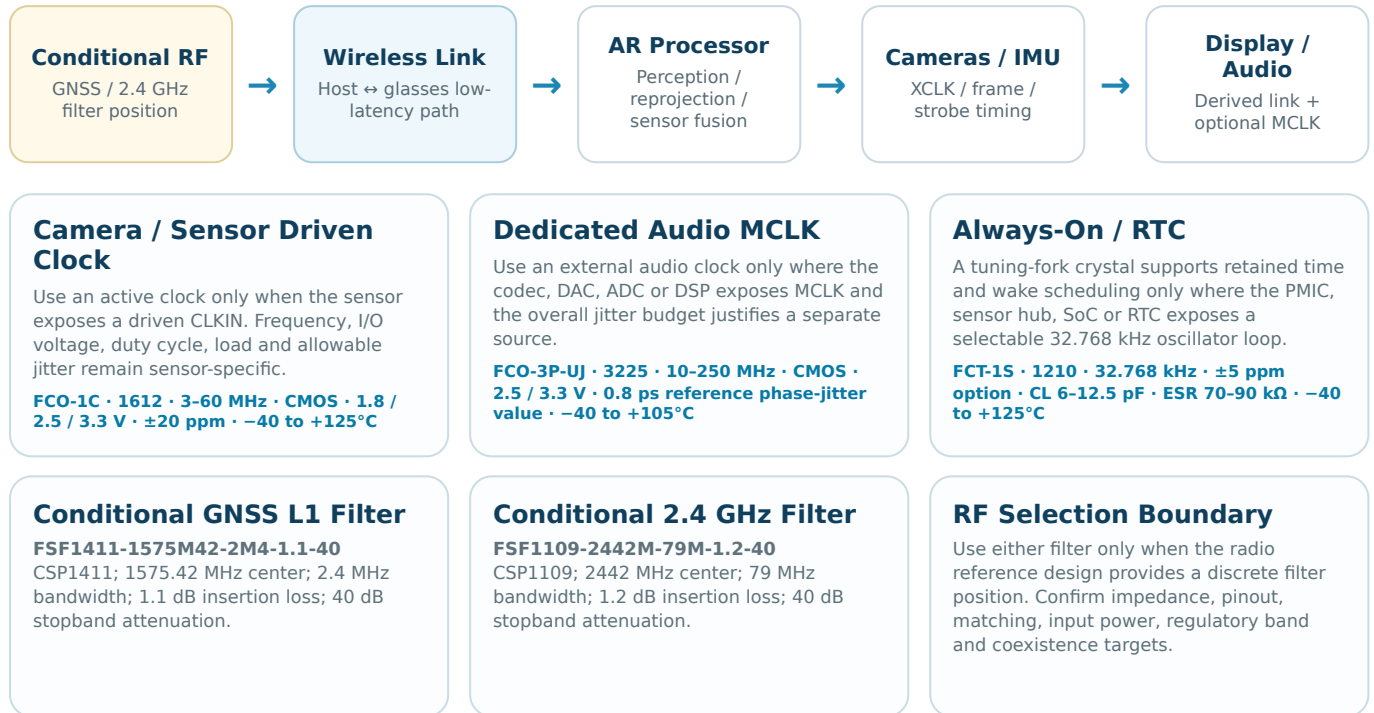


Architecture note: the main XR processor reference, 24 MHz display reference and 100 MHz-class high-speed REFCLK are separate nodes. These nodes should be evaluated independently, even when a clock generator or SoC contains internal PLLs.

06

Distributed Smart-Glasses & Perception Architecture

Representative timing around the host link, on-glass processing, camera / sensor domains, audio, retained-time and conditional RF filtering.



Architecture note: a wireless or GNSS module may already integrate its reference and RF filtering. An external host-board oscillator or SAW filter is appropriate only when the module documentation defines the corresponding interface.

07

FCom Selection Guidance by Design Condition

The selections below are limited to clock and RF positions where the target architecture creates a clear component decision. Exact ordering configurations are confirmed after the receiving interface is defined.

Miniature XTAL

Compact processor, radio, display-controller or sensor oscillator loop.

Driven CMOS

Camera, bridge or audio node with a documented CLKIN.

Low-Jitter Differential

PCIe / FPGA / SerDes receiver with an explicit jitter mask.

Conditional RF

GNSS or 2.4 GHz front end with a defined discrete-filter position.

Design Condition	FCom Selection	Published Series Specifications	Key Check Before RFQ
24-76.8 MHz + smallest passive footprint	FCX-1S	1210 4-SMD; ± 5 ppm tolerance option; ± 10 ppm stability option; -40 to $+125^{\circ}\text{C}$; specified CL available.	Exact frequency · CL · ESR · drive · startup
24 MHz display-controller oscillator loop	FCX-2S	2016 4-SMD; 16-96 MHz; ± 5 / ± 10 ppm options; -40 to $+125^{\circ}\text{C}$; specified CL; ESR 30-100 Ω by frequency.	Receiver's 6 pF / ESR / startup limits and margin test
3-60 MHz driven sensor / bridge clock	FCO-1C	1612 4-SMD; CMOS; 1.8 / 2.5 / 3.3 V; ± 20 ppm; -40 to $+125^{\circ}\text{C}$.	CLKIN support · VDD · load · duty cycle · OE
100-220 MHz + differential + low jitter	FCO-2L-UJ	2520 6-SMD; LVPECL / LVDS / HCSL; 1.8 / 2.5 / 3.3 V; ± 20 ppm; -40 to $+125^{\circ}\text{C}$; 50 fs reference phase-jitter value.	Output logic · termination · jitter band · receiver mask
Dedicated CMOS audio / peripheral MCLK	FCO-3P-UJ	3225 6-SMD; 10-250 MHz; CMOS; 2.5 / 3.3 V; ± 25 ppm; -40 to $+105^{\circ}\text{C}$; 0.8 ps reference phase-jitter value.	Exact MCLK · jitter budget · integration band · load
32.768 kHz XTAL-input retained-time	FCT-1S	1210 2-SMD; ± 5 ppm option; CL 6-12.5 pF; ESR 70-90 k Ω ; -40 to $+125^{\circ}\text{C}$.	Oscillator-loop CL / ESR · backup power · startup
Defined GNSS L1 or 2.4 GHz RF filter position	FSF1411-1575M42-2M4-1.1-40 FSF1109-2442M-79M-1.2-40	1575.42 MHz / 2.4 MHz BW / 1.1 dB IL / 40 dB; or 2442 MHz / 79 MHz BW / 1.2 dB IL / 40 dB.	Impedance · pinout · matching · power · RF mask

Selection boundary: low-power XO, TCXO / VCTCXO, spread-spectrum clock and other FCom classes are evaluated when required by the receiving device or system-level specification, rather than as default elements of an XR platform.

ENGINEERING SELECTION SUPPORT

Request an FCom XR Timing Recommendation

Provide the target SoC, display controller, camera, wireless IC, codec, bridge, PCIe receiver or RF front-end part number together with its clock / filter interface and operating requirements.

[Start Engineering Review →](#)

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Engineering Validation & Minimum RFQ

XR timing is defined by the receiving device, clock topology, latency objective and complete electrical environment—not by nominal frequency alone.

Compute / Wireless

- Exact SoC / PMIC / radio part number
- Chip-down or module boundary
- XTAL pins or driven CLKIN
- Frequency, CL / ESR or VDD / logic
- Accuracy, startup and power state

Display / Camera

- Display controller / sensor P/N
- Reference-clock and frame-sync pins
- Exact XCLK / MOSC frequency
- Crystal or driven-clock topology
- Multi-camera skew / trigger objective

High-Speed / Audio

- PCIe / bridge / FPGA / codec P/N
- HCSL / LVDS / LVPECL / CMOS
- Frequency and termination
- RMS jitter and integration band
- Audio MCLK family and clock switching

RTC / RF Front End

- RTC XTAL or external CLKIN
- CL / ESR or VDD / current
- GNSS / Wi-Fi / Bluetooth architecture
- Required center / bandwidth / loss / rejection
- Impedance, matching and antenna path

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	XR SoC, wireless IC, display controller, camera, sensor hub, codec / DAC, PCIe / bridge, RTC or RF front-end filter.
Target Device	Exact receiving IC or module part number, clock / RF pin and schematic location.
Clock Topology	External crystal, local CMOS XO, module-integrated reference, shared clock, differential REFCLK or 32.768 kHz timebase.
Crystal Requirements	Frequency, package, CL, ESR, tolerance / stability, drive level, startup and operating temperature.
XO Requirements	Frequency, VDD, output logic, load, OE, duty cycle, stability, phase jitter / noise and integration band.
RF Filter Requirements	Center frequency, bandwidth, insertion loss, rejection mask, impedance, pinout, matching, input power and antenna architecture.
Program Requirements	Prototype quantity, sample date, validation plan, annual volume, production site, lifecycle and compliance documentation.

Module Boundaries Matter

An internal crystal or SAW filter belongs to the module implementation unless a documented external reference or RF interface is provided.

Multi-Camera Timing Is a System Problem

XCLK quality, frame triggers, sensor latency, ISP capture and software timestamps must be evaluated together.

Interface Rate Is Not REFCLK

MIPI, USB, PCIe and display data rates do not directly identify the board-level oscillator.

Frequency alone does not define the final part: the receiving device, topology, output interface, power state and validated jitter / RF mask determine the appropriate FCom configuration.

09

Engineering FAQ & Application Review

Common XR clock-selection questions, representative public references and the information required for an FCom engineering recommendation.

Is the XR processor frequency the external crystal frequency?

No. CPU, GPU and DSP operating clocks are normally synthesized internally from one or more platform references.

Does 90 / 120 Hz display refresh define the oscillator?

No. Refresh rate is part of the display pipeline. The display controller or panel reference must be taken from its own documentation.

Does MIPI lane rate identify camera XCLK?

No. MIPI is the output-link rate. Sensor XCLK, exposure timing and frame synchronization are separate parameters.

Can one 24 MHz crystal be reused across every node?

Not automatically. Each oscillator loop has its own CL, ESR, drive, startup and PCB-parasitic requirements.

When is a low-jitter differential XO appropriate?

When a PCIe, FPGA, bridge or SerDes receiver specifies a differential REFCLK and a defined RMS-jitter mask.

When is an external audio XO justified?

Only when the codec, DAC, ADC or DSP exposes MCLK and the complete audio clock tree requires a dedicated source.

What is 32.768 kHz used for?

RTC, wake scheduling and retained-time functions where the selected SoC, PMIC, sensor hub or RTC exposes an external low-frequency input.

Is a GNSS or 2.4 GHz SAW filter always required?

No. It is used only when the selected RF architecture provides a discrete filter position and the device matches the required RF mask.

Representative Public Technical References

1. **Qualcomm:** Snapdragon AR2 Gen 1 — distributed processing, camera and low-latency wireless architecture.
2. **Qualcomm:** Snapdragon XR2+ Gen 2 — integrated VR / MR compute, display and multi-camera architecture.
3. **Thundercomm:** TurboX C865C SOM — public AR/VR display, camera, wireless and high-speed I/O interfaces.
4. **Texas Instruments:** DLPC3430 / DLPC3435 data sheet — 24 MHz reference requirements and crystal configuration.
5. **OMNIVISION:** OG0VE — global-shutter AR/VR perception sensor architecture and publicly documented capabilities.
6. **Nordic Semiconductor:** nRF5340 oscillator documentation — 32 MHz HFXO and 32.768 kHz LFXO examples.
7. **Texas Instruments:** CDCM9102 — 25 MHz crystal input and dual 100 MHz PCIe clock outputs.
8. **Qorvo:** DWM3000 — UWB module with integrated crystal, illustrating the module-internal timing boundary.

FCom product specification note: product information in this guide is presented at series or representative-configuration level unless a complete SAW filter P/N is shown. Exact ordering codes, guaranteed limits and availability are confirmed against the applicable FCom specification and quotation.

ENGINEERING REVIEW

AR/VR & Spatial Device Timing Review

Provide the target processor, display controller, camera, wireless IC, codec, bridge, PCIe receiver, RTC or RF front-end part number together with its clock / filter interface, frequency, electrical limits, operating temperature, package and project stage.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.