

AI DATA CENTERS, SERVERS & ACCELERATORS

AI Data Centers, Servers & Accelerators

Coordinate host, accelerator, PCIe / CXL, high-speed fabric and management timing across AI servers, GPU / ASIC platforms and data-center acceleration hardware.

AI Compute + PCIe / CXL + Accelerator Fabric + High-Speed I/O + Management / RTC

AI Training Servers

GPU / ASIC Accelerators

PCIe Gen5 / Gen6

CXL

HBM Platforms

400G / 800G Fabric

BMC / RTC

Application Scope

GPU and ASIC servers, accelerator baseboards, PCIe add-in cards, adaptive-compute platforms, CXL endpoints, retimers, DPUs, high-speed NICs and management subsystems.

Selection Philosophy

Selection begins with the physical receiving clock node. Core frequency, memory data rate and network line rate are not substitutes for the documented external reference-clock requirement.

Host & Root Complex

CPU platform, PCIe root ports, clock distribution and system management.

Accelerator Fabric

GPU, ASIC, FPGA, NVLink-class or Ethernet-based scale-up domains.

PCIe / CXL

Common Clock, SRNS / SRIS and local low-jitter reference architectures.

High-Speed I/O

SerDes, NIC, DPU, retimer and optical-interface reference clocks.

01

Application Scope & Engineering Domains

AI compute platforms combine host, accelerator, memory, fabric and management functions, each with a different clock-source role.

One server, multiple clock architectures. A 100 MHz PCIe reference, 33.333333 MHz board reference, 156.25 MHz SerDes reference and 32.768 kHz RTC source can coexist on one platform without being interchangeable.

Typical Equipment

AI Compute Systems

GPU Training Server
Inference Server
HGX / OAM Baseboard
HPC Compute Node
AI Appliance

Accelerator Hardware

GPU / ASIC Accelerator
Adaptive Accelerator Card
FPGA Accelerator
PCIe Add-In Card
Retimer / Switch Board

Memory & Fabric

CXL Endpoint / Expander
HBM / DDR Platform
DPU / SuperNIC
400G / 800G Interface
Optical DSP / Module

Five Engineering Domains

Host / Processor

CPU root complex, chipset, BMC and board-level reference domains.

PCIe / CXL

100 MHz clock topology, SSC, electrical mask and generation-specific jitter.

Accelerator / FPGA

Local system clocks, transceiver references and programmable clock trees.

Fabric / Optical

SerDes, retimer, Ethernet, QSFP-DD and optical DSP reference clocks.

Physical Clock Role

Crystal loop, local XO, host-supplied REFCLK or clock-generator output.

Output & Mask

CMOS, HCSL / LP-HCSL, LVDS, LVPECL, amplitude and termination.

Jitter / SSC

RMS integration band, PCIe mask, phase-noise profile and SSC mode.

Lifecycle / Thermal

Package, airflow, operating temperature, qualification and production status.

Generated-frequency boundary: HBM clocks, accelerator core clocks, PCIe user clocks and many 200 / 300 / 322.265 MHz domains are generated inside clock ICs or silicon. Treat them as internally generated domains unless the design documents a physical external-clock input.

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Select by System Node First

Begin with the receiving pin, then determine whether the requirement is a resonator, driven clock, host REFCLK or generated output.

System Node	Clock Role	Representative Frequency	Required Device Class	Selection Route	Selection Focus
BMC / RTC	Retained time, timestamp and always-on domain	32.768 kHz	Tuning-fork crystal or low-current CMOS XO	Choose by XTAL pins or driven CLKIN	CL / ESR or VDD / current · backup-power behavior
BMC / Clock Generator	Local crystal-loop input	25 / 33.333 / 38.4 / 50 MHz	Passive MHz crystal	Match the receiver's oscillator loop	Receiver CL · ESR · drive level · startup margin
Management / Auxiliary Logic	Locally driven CMOS reference	33.333333 / 38.4 / 50 / 75 MHz	CMOS SPXO	Select after voltage and load are known	VDD · logic threshold · OE · load · temperature
PCIe / CXL Root or Endpoint	Common, local or independent REFCLK	100 MHz	HCSSL / LP-HCSSL low-jitter clock	Confirm that a local source is required	PCIe generation · SSC · topology · mask · termination
FPGA / Accelerator System Ref	Differential reference or MGT REFCLK	125 / 156.25 / 161.1328125 MHz	LVDS / LVPECL / HCSSL low-jitter XO	Qualify by interface and jitter budget	Exact logic · integration band · receiver load
QSFP-DD / SerDes	Transceiver-bank reference	156.25 / 322.265 / 325.50 MHz	Low-jitter differential XO or clock-generator output	Separate discrete source from generated output	PHY mode · line rate · jitter ceiling · output swing
Optical DSP / Emerging I/O	High-frequency differential reference	312.5 / 625 MHz	High-frequency differential source	Submit receiver requirements for engineering review	Frequency, jitter and phase noise must all fit the receiver
HBM / DDR / User Clock	Clock-generator or silicon-derived output	200 / 300 MHz class	Generated domain	No standalone XO by default	Confirm physical source before selecting a component

1 · Identify the Receiver

Record the exact CPU, GPU, FPGA, BMC, retimer, NIC, DPU or optical-DSP clock pin.

Start from the node, not the headline frequency.

2 · Classify the Clock Domain

Separate passive crystal loops, local oscillators, host-supplied clocks and generated outputs.

Treat a clock-IC output as a separate oscillator input only when the architecture explicitly requires one.

3 · Apply Electrical Constraints

Confirm output logic, voltage, SSC, RMS jitter band, termination, load and operating temperature.

Frequency coverage alone is not qualification.

Recommended sequence: system node → receiving clock pin → source topology → frequency → output logic → jitter / SSC → voltage → temperature → package → lifecycle.

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Frequency & Component Placement Matrix

Frequency becomes meaningful only when it is tied to a documented physical clock source, receiving interface and electrical mask.

Frequency	Typical Physical Node	Source Topology	Recommended Device Direction	Engineering Boundary
32.768 kHz	BMC, RTC, service processor, always-on controller	Crystal loop or driven low-current CMOS	RTC crystal or low-current CMOS oscillator	Crystal CL / ESR and oscillator current are separate selection paths.
33.333333 MHz	Adaptive accelerator board system reference	Local LVCMOS oscillator or clock-buffer input	CMOS SPXO when a discrete source is documented	Confirm LVCMOS voltage, duty cycle, load and whether the public platform uses a discrete XO.
38.4 / 50 / 75 MHz	BMC, controller, programmable clock IC or auxiliary logic	Crystal loop or CMOS SPXO	Passive crystal or CMOS SPXO, topology dependent	Do not confuse management clocks with PCIe or accelerator fabric references.
100 MHz	PCIe Gen5 / Gen6 and CXL root, endpoint, switch or retimer	Host Common Clock, local clock or independent clock	Low-jitter HCSL / LP-HCSL only for a local source	HCSL label alone is insufficient; generation mask, SSC architecture and termination must be validated.
125 MHz	FPGA, NIC, board reference and selected Ethernet domains	CMOS or differential SPXO	CMOS or low-jitter differential XO	Output logic and jitter budget determine the product class.
156.25 / 161.1328125 MHz	SerDes, MGT, Ethernet, Aurora-class or platform-specific reference	Differential local XO or clock-generator output	Low-jitter differential XO when externally sourced	These frequencies are not interchangeable; match the exact PHY / platform value.
200 / 300 MHz	HBM, DDR controller and PCIe user-clock domains	Usually generated by a clock IC or PLL	Generally not a standalone-XO requirement	Verify that the frequency exists at a physical oscillator input before requesting a component recommendation.
312.5 / 322.265 / 325.50 MHz	High-speed Ethernet, QSFP-DD, optical or FPGA transceiver bank	High-frequency differential XO or clock generator	FCom engineering review required before recommendation	Agilex public guidance specifies <250 fs for its 325.50 MHz PAM4 clock; frequency coverage alone is insufficient.
625 MHz	Emerging 800G / 1.6T optical DSP and high-rate SerDes reference	High-performance differential source	Receiver-specific engineering review required	Provide the exact jitter, phase-noise, swing and lifecycle specification before product selection.

32.768 kHz
 RTC / BMC retained-time domain.

100 MHz
 Primary PCIe / CXL external reference class.

156.25 MHz
 High-value differential SerDes reference.

325.50 / 625 MHz
 Platform-specific, receiver-qualified reference domains.

Selection rule: “available from a series” is not the same as “qualified for an interface.” The receiving device, electrical standard, SSC architecture and specified jitter integration method remain the release criteria.

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Representative Platform & Architecture Matrix

Four public platforms illustrate GPU scale-up, Ethernet-based acceleration, adaptive-compute cards and PCIe / CXL prototyping.

NVIDIA

01

HGX B300 Baseboard / AI Factory Node

Public architecture: eight B300 GPUs, fifth-generation NVLink / NVSwitch, eight PCIe Gen5 x16 links, eight ConnectX-8 SuperNICs and one BlueField-3 DPU per server.

Clock interpretation: PCIe Gen5 creates a 100 MHz-class reference domain, but NVIDIA does not publish the oscillator BOM or board clock tree in the system-level reference architecture.

Selection insight: FCom can support timing selection at the ODM baseboard, NIC, DPU, retimer or optical-interface board level after the physical clock interface is defined.

Host / PCIe → GPU / NVLink → 800G Fabric

INTEL

02

Gaudi 3 HLB-325 Accelerator Baseboard

Public architecture: eight Gaudi 3 OAM accelerators with direct all-to-all connectivity; each accelerator integrates HBM2e and multiple 200 Gb Ethernet ports for scale-up and scale-out.

Clock interpretation: host PCIe and Ethernet SerDes references are separate domains. The public brief does not disclose their exact board frequencies, output formats or oscillator identities.

Selection insight: the PCIe and Ethernet receiver specifications should be confirmed from the HLB schematic or target-device documentation before a timing component is selected.

Host Interface → 8× Gaudi 3 → Ethernet Scale-Out

AMD

03

Alveo V80 Data Center Accelerator

Public architecture: PCIe Gen4 x16 or dual Gen5 x8, Versal HBM adaptive SoC, HBM2e, DDR4, four QSFP56 ports and MCIO PCIe expansion.

Published clocks: 33.333333 MHz LVCMOS18 board reference; 100 MHz host PCIe REFCLK; generated 200 MHz LVDS memory clocks and 322.265 MHz QSFP56 references.

Selection insight: 33.333333 MHz is the documented discrete-XO position; 100 MHz is host supplied, while 200 / 322.265 MHz are clock-generator outputs.

33.333333 XO → Versal / HBM → QSFP56

ALTERA

04

Agilex 7 I-Series Development Kit

Public architecture: dual PCIe / CXL 5.0 x16 paths through R-Tiles, MCIO expansion, dual QSFP-DD through F-Tile and DDR4 ECC memory.

Published clocks: selectable local / edge PCIe clocking, 50 MHz management clock, 156.25 MHz for 28G NRZ and 325.50 MHz for 56G PAM4; the transceiver reference requires RPM jitter below 250 fs.

Selection insight: 156.25 MHz represents a conventional low-jitter differential-XO node; 325.50 MHz requires a separate high-frequency performance review.

PCIe / CXL → Agilex R/F-Tile → QSFP-DD

Platform interpretation: public architecture establishes where clocks exist, but it does not establish an AVL. Only AMD V80 and the Agilex development kit expose enough board-level clock detail to distinguish discrete sources from clock-generator outputs.

05

AI Server Host + Accelerator Timing Architecture

Representative clock placement around the host platform, PCIe / CXL fabric, accelerator endpoints and data-center I/O.

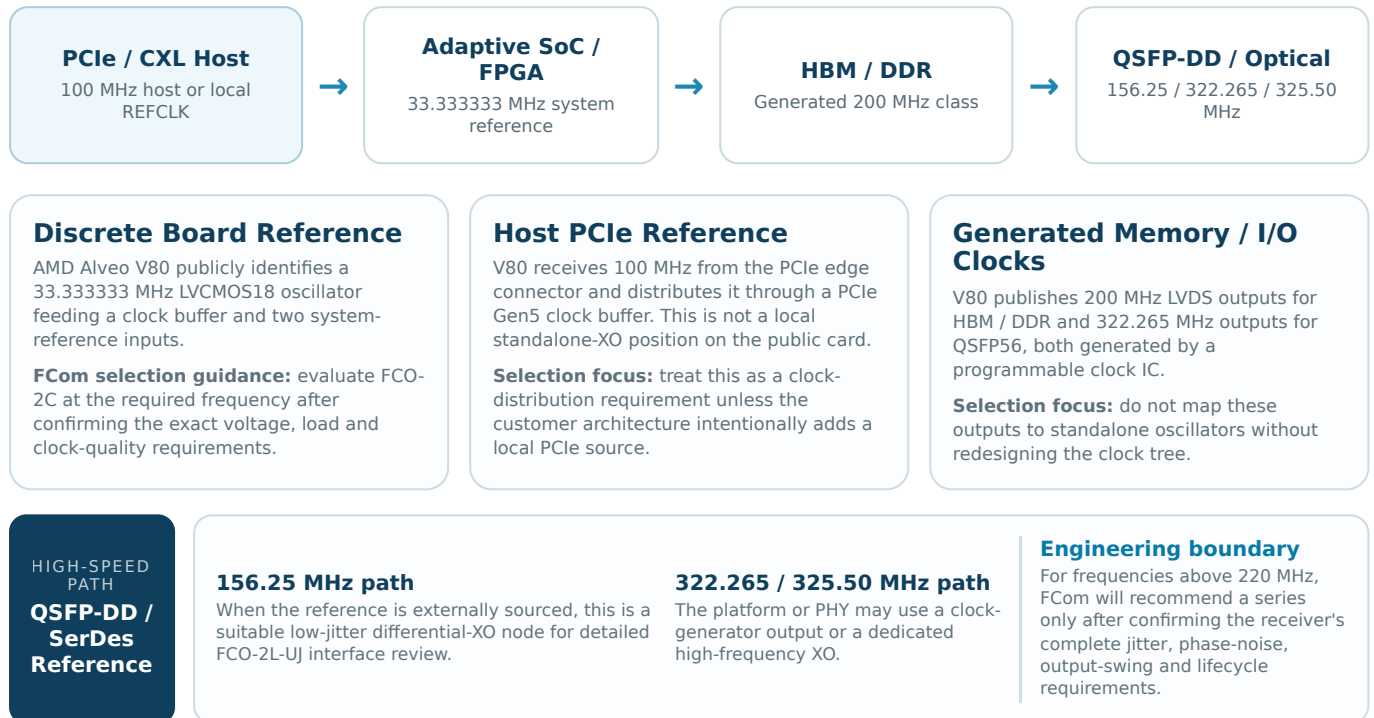


Architecture note: a finished NVIDIA or Intel AI server does not expose its oscillator AVL in the public system guide. FCom selection therefore occurs at the ODM board, accelerator card, DPU, NIC, retimer or optical-interface design level.

06

Adaptive Accelerator + HBM + High-Speed I/O

Representative timing around a PCIe accelerator card that combines adaptive compute, memory and QSFP-class interfaces.



Architecture note: the component-selection point for an external oscillator is the source entering the clock tree, not every frequency leaving the clock generator. This distinction prevents generated HBM, DDR and QSFP clocks from being misidentified as standalone XO inputs.

07 FCom Selection Guidance by Design Condition

The following FCom families are shown only for system nodes with a defined physical clock input. Exact ordering codes are confirmed after the frequency and electrical configuration are established.

RTC / BMC Crystal
32.768 kHz retained-time resonator input.

Driven Board Reference
33.333333-125 MHz local CMOS CLKIN.

Low-Jitter Differential
100-220 MHz HCSL / LVDS / LVPECL reference.

High-Frequency Review
Above 220 MHz: receiver-level qualification before recommendation.

Design Condition	FCom Selection	Published Matrix Capability	Key Check Before RFQ
RTC exposes 32.768 kHz XTAL pins	FCT-1M	1610 2-SMD; 32.768 kHz; ± 5 ppm; -40 to +125 °C; CL 6-12.5 pF; ESR 70-90 k Ω .	RTC IC · CL · ESR · drive · startup · backup power
RTC / BMC expects driven 32.768 kHz CLKIN	FCO-6K-UC	2016 4-SMD CMOS; 1.5 / 1.8 V; ± 20 ppm; -40 to +105 °C; 1.4-1.8 μ A.	CLKIN amplitude · supply · current · OE / startup
BMC / clock generator exposes a passive 24-60 MHz crystal loop	FCX-1M	1612 4-SMD; 24-60 MHz; ± 5 ppm tolerance; ± 10 ppm stability; -40 to +125 °C; CL 18 pF or specified; ESR 30-60 Ω .	Receiver CL · ESR · drive level · startup margin
Board node expects local CMOS CLKIN	FCO-2C	2520 4-SMD CMOS; 1.25-125 MHz; 1.8 / 2.5 / 3.3 V; ± 20 ppm; -40 to +125 °C.	Exact frequency · voltage · CMOS load · OE · duty cycle
100-220 MHz + differential + explicit low jitter	FCO-2L-UJ	2520 6-SMD; HCSL, LVDS or LVPECL; 1.8 / 2.5 / 3.3 V; ± 20 ppm; -40 to +125 °C; 50 fs matrix jitter.	Output variant · jitter band · PCIe mask · SSC · termination

Product-boundary note: FCom reviews package alternatives after the electrical target is established. For frequencies above 220 MHz, or where tuning, synchronization or holdover is required, FCom engineering will recommend a series only after the receiver requirements are confirmed. Crystal filters, SAW resonators and SAW filters serve RF / IF functions and are outside the AI compute clock path.

ENGINEERING SELECTION SUPPORT

Request an FCom AI Platform Timing Recommendation

Provide the target CPU / GPU / ASIC / FPGA / BMC / retimer / NIC / optical-DSP part number, physical clock pin, source topology, frequency, output logic, jitter / SSC requirement, voltage, temperature, package and project stage.

Start Engineering Review →



Engineering Validation & Minimum RFQ

AI-platform timing is defined by the physical receiver, clock topology, interface generation and system environment in addition to frequency.

BMC / Management

- Exact BMC / RTC / service-processor P/N
- XTAL pins or driven CLKIN
- 32.768 kHz CL / ESR or VDD / current
- Main reference frequency and logic
- Backup-power architecture
- Operating temperature

PCIe / CXL

- Root port, endpoint, switch or retimer P/N
- PCIe / CXL generation
- Common Clock, SRNS or SRIS
- SSC enabled / disabled and source location
- HCSL / LP-HCSL electrical mask
- Jitter and termination requirements

Accelerator / FPGA

- GPU / ASIC / FPGA / adaptive-SoC P/N
- Exact REFCLK or MGT input
- Local XO, host clock or clock-generator output
- Frequency, voltage and output logic
- RMS-jitter integration band
- Airflow, temperature and lifecycle

Fabric / Optical I/O

- NIC / DPU / retimer / PHY / DSP P/N
- Ethernet / InfiniBand / optical mode
- Lane rate and encoding
- 156.25 / 312.5 / 322.265 / 325.50 / 625 MHz
- Phase-noise or jitter mask
- Output swing and termination

Minimum RFQ Information

Information Category	What to Provide
Application / System Node	AI server motherboard, accelerator baseboard, PCIe card, CXL endpoint, FPGA, DPU, NIC, retimer, optical DSP or BMC / RTC.
Target Device	Exact receiving IC part number and physical clock pin / schematic location.
Clock Topology	Crystal loop, local CMOS XO, host Common Clock, SRNS / SRIS, clock buffer, clock-generator output or driven RTC source.
Electrical Requirements	Frequency, VDD, CMOS / HCSL / LP-HCSL / LVDS / LVPECL, load, swing, termination, OE and startup behavior.
Performance Requirements	Stability, temperature, RMS-jitter integration band, phase-noise mask, SSC profile and interface compliance target.
Program Requirements	Prototype quantity, sample date, validation plan, annual volume, production location, lifecycle and compliance documentation.

100 MHz Does Not Define the Part

A 100 MHz node may be host supplied, local HCSL, independent SRIS or a buffered Common Clock path.

156.25 MHz Can Use Different Outputs

FPGA, Ethernet and optical interfaces may request LVDS, LVPECL, HCSL or a clock-generator output.

625 MHz Is Performance-Gated

Frequency coverage is not sufficient; current 800G / 1.6T designs may require extremely low jitter and a specific output swing.

Frequency alone does not define the final part: a complete recommendation requires the source architecture, electrical mask, jitter measurement method and receiver-specific operating conditions.

09

Engineering FAQ & Application Review

Common AI-platform timing questions, representative public architecture references and the information required for FCom engineering review.

Is the GPU or accelerator core frequency supplied by the external XO?

No. The external reference feeds a PLL or clock-management domain; multi-gigahertz core clocks are generated inside the processor or accelerator.

Is every PCIe 100 MHz reference a local oscillator?

No. It may originate at the host, pass through a buffer, use Common Clock distribution or be locally generated for an independent-clock architecture.

Can a 100 MHz CMOS oscillator replace a 100 MHz HCSL source?

No. CMOS and HCSL use different electrical interfaces, swings, loading and compliance requirements.

Does CXL require a separate nominal frequency from PCIe?

CXL uses the PCIe physical infrastructure, but the endpoint, topology, generation, SSC and clock-distribution requirements must still be confirmed.

Does 800G Ethernet imply an 800 MHz oscillator?

No. Ethernet line rate and external reference frequency are different layers of the PHY / SerDes architecture.

Are 322.265 and 325.50 MHz interchangeable?

No. They are platform- and PHY-specific reference frequencies and must match the documented receiver value.

Can a high-frequency XO be selected by frequency range alone?

No. Jitter integration band, phase-noise profile, output swing, receiver mask and lifecycle must be accepted together.

When are TCXO or OCXO products relevant?

They become application-specific options when the platform defines precision synchronization, frequency holdover, tuning or unusually tight absolute accuracy.

Representative Public Technical References

1. **NVIDIA:** HGX B300 AI Factory components and system architecture.
2. **Intel:** Gaudi 3 HLB-325 accelerator baseboard product brief.
3. **Intel:** Gaudi 3 compute, HBM and 200 Gb Ethernet architecture.
4. **AMD:** Alveo V80 board clock tree and published reference frequencies.
5. **AMD:** Alveo V80 architecture, PCIe, HBM and QSP56 interfaces.
6. **Altera:** Agilex 7 I-Series development-kit clock circuits.
7. **Altera:** dual PCIe / CXL 5.0 x16 platform architecture.
8. **Altera:** 156.25 / 325.50 MHz transceiver references and <250 fs jitter requirement.

FCom product specification note: product information in this guide is presented at series or representative-configuration level from the supplied in-sale matrix. Exact ordering codes, guaranteed limits, frequency availability and interface compliance are confirmed against the applicable FCom specification and quotation.

ENGINEERING REVIEW

AI Server & Accelerator Timing Review

Provide the exact receiver, clock pin, topology, frequency, supply, output logic, SSC mode, jitter / phase-noise target, temperature, package and project stage. FCom can review the requirement and recommend an appropriate timing series and configuration for board and system validation.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.