

ADAS & SENSOR FUSION

ADAS, Cameras & Sensor Fusion

Control clock jitter across cameras, radar, SerDes, FPGA and sensor-processing interfaces to support reliable high-speed data acquisition and sensor-fusion paths.

Sensor Clocking + SerDes Timing + Radar Reference + Low-Jitter REFCLK + Sensor Fusion

Vehicle Cameras

77–81 GHz Radar

FPD-Link / SerDes

ADAS SoC

FPGA / Adaptive SoC

Automotive Ethernet

Application Scope

Camera modules, radar sensors, serializer / deserializer links, sensor hubs, ADAS processors, FPGA / adaptive compute and high-speed network interfaces.

Selection Philosophy

Select by clock node and topology first. Determine whether the clock is locally generated, forwarded, recovered or externally distributed before assigning a crystal or oscillator.

Camera

Image-sensor XCLK, camera controller and serializer references.

Radar

Radar SoC / RF front-end external timing references.

SerDes

Serializer / deserializer, clock forwarding and sensor transport.

Fusion Compute

SoC / FPGA / PCIe / Ethernet high-speed processing references.

01

Application Scope & Engineering Domains

Separate sensor acquisition, transport, processing and high-speed interface timing before selecting the external reference device.

ADAS timing is a multi-domain problem. A camera sensor, radar SoC, SerDes link and fusion processor can each use a different clock architecture. External timing selection therefore begins with the receiving device specification and its documented clock input, rather than with pixel rate, RF carrier frequency or interface data rate.

Typical Equipment

Camera & Vision

Front Camera
Surround View / AVM
Driver Monitoring
E-Mirror / CMS
Camera ECU

Radar & Sensor Transport

Corner Radar
Front Radar
Radar ECU
Serializer / Deserializer
Multi-Sensor Hub

Fusion & Compute

ADAS SoC
ISP / AI Accelerator
FPGA / Adaptive SoC
Domain Controller
High-Speed Ethernet / PCIe

Five Engineering Domains

Camera Timing

Sensor master clock, local crystal / XO, serializer and ISP reference.

Radar Timing

Radar SoC / RF front-end external reference; RF and sampling clocks are internally synthesized.

SerDes Timing

Local, forwarded and recovered clock paths through serializer / deserializer links.

Processing Timing

ADAS SoC / FPGA / PCIe / Ethernet reference clocks for sensor-fusion processing.

RMS Jitter

Critical at FPGA / PCIe / Ethernet / SerDes high-speed REFCLK nodes.

Frequency Accuracy

Tolerance, temperature stability and interface ppm budget.

Clock Topology

XTAL · CLKIN · forwarded · recovered · differential REFCLK.

Environment

AEC qualification · local PCB temperature · startup · vibration / EMC.

Clock-definition note: camera pixel clock, MIPI CSI-2 lane rate, FPD-Link line rate, 76–81 GHz radar RF, radar chirp, ADC sample rate, CPU / DSP frequency, PCIe lane rate and Ethernet line rate belong to internal or interface timing domains and should be distinguished from the external reference clock.

02

Select by System Node First

Begin with the receiving device and its clock topology—local, forwarded, recovered or externally distributed—then select the required frequency and device class.

System Node	Clock Role	Representative External Reference	Typical Device	Selection Focus
Image Sensor	Sensor master clock / XCLK	24 / 27 MHz 16 / 30 MHz platform-dependent	Crystal / CMOS XO	Local vs forwarded clock, ppm, jitter, startup, package
Serializer / Deserializer	Sensor transport reference	25 / 27 / 50 MHz class	Crystal / CMOS XO / recovered clock	Clock forwarding, local reference, link mode, clock output
Radar SoC / RF Front End	Radar external reference	40 MHz 20 / 50 MHz platform-dependent	Crystal / CMOS XO	Oscillator interface, accuracy, phase noise if specified, temperature
ADAS SoC / Processor	Processor PLL reference	19.2 / 20 / 24 / 25 / 27 / 40 MHz class	Crystal / CMOS XO	PLL input, clock distribution, thermal zone
FPGA / PCIe / High-Speed SerDes	High-speed REFCLK	100 / 125 / 156.25 MHz	Low-jitter CMOS / differential XO	RMS jitter, output logic, termination, signal integrity
RTC / Event Time	Retained-time reference	32.768 kHz	Tuning-fork crystal / kHz XO	RTC topology, CL / ESR, standby current

1 · Determine Clock Ownership

Is the clock generated locally at the sensor, forwarded through SerDes, recovered from the link or distributed from a central clock source?

2 · Separate Standard vs High-Speed

24 / 25 / 27 / 40 MHz sensor / controller references follow crystal or CMOS-XO criteria; 100 / 125 / 156.25 MHz high-speed REFCLK adds jitter and output-logic constraints.

3 · Apply Automotive Constraints

Confirm operating temperature, qualification, package, startup margin and signal-integrity requirements before selecting the FCom series.

Recommended sequence: System node → clock ownership → XTAL / CLKIN / differential input → frequency → jitter / phase-noise requirement → qualification / temperature → package → FCom series → final electrical configuration.

03

Frequency & Component Placement Matrix

The same frequency can serve different nodes. Classify it by system position and interface before selecting a timing device.

Frequency	Representative System Position	Applicability	Selection Interpretation
32.768 kHz	RTC / Event Time / Retained-Time	Secondary External Reference	Use where the RTC / supervisor provides an external low-speed oscillator node.
16 / 19.2 / 20 MHz	Image sensor / radar / processor reference	Platform-Dependent	Confirm the exact sensor / SoC oscillator interface.
24 MHz	Image sensor XCLK / camera / processor	Common External Reference	Frequently used as driven sensor or processor reference.
25 MHz	Camera SerDes / Ethernet / processor	Common External Reference	May be local crystal / XO or part of a forwarded-clock architecture.
27 MHz	Image sensor / camera / SerDes	Common External Reference	Appears in both crystal-input and driven-clock sensor paths.
30 / 33.33 MHz	Image sensor / automotive computer	Platform-Dependent	Application-specific sensor or processor reference.
40 MHz	Automotive radar / radar SoC / processor	Common Radar Reference	TI AWR2944 publicly supports 40 MHz crystal, oscillator or driven clock.
50 MHz	SerDes / radar / processor / network	Interface-Dependent	Use only where the selected interface specifies a 50 MHz local / driven reference.
100 / 125 / 156.25 MHz	FPGA / PCIe / Ethernet / High-Speed SerDes	High-Speed Extension	Low-jitter CMOS or differential reference; output logic and jitter become first-order requirements.

Often Internally Derived — Do Not Treat as External Crystal Frequency

Camera
Pixel clock · frame rate · MIPI CSI-2 lane rate

SerDes
FPD-Link / GMSL line rate · recovered high-speed clocks

Radar
76–81 GHz RF · chirp bandwidth · ADC sample rate

Compute
CPU / DSP clock · PCIe lane rate · Ethernet line rate

Jitter boundary: standard camera / radar controller clocks are normally selected from frequency, startup and stability requirements. Explicit RMS-jitter and differential-output requirements become more significant at FPGA, PCIe, Ethernet and high-speed SerDes REFCLK nodes.

04

Representative Platform & Architecture Matrix

Four public platforms illustrate sensor transport, radar timing, multi-sensor fusion and high-speed adaptive-compute clock domains. These examples are used as architecture evidence only.

TEXAS INSTRUMENTS

1

TIDA-01413 · 8-Channel Camera + Radar Sensor Fusion Hub

Architecture: up to four 2-MP cameras and four radar modules connect through coax to two 4-Gbps FPD-Link III quad deserializers, with dual MIPI CSI-2 outputs to an application processor.

Clock evidence: TI states that the coax links provide power, back-channel communication and **clock synchronization** to the sensors.

Camera / Radar → FPD-Link III → Deserializer Hub / CSI-2

Selection insight: the sensor clock topology—local, forwarded or recovered—determines whether a dedicated timing device is required at a given node.

TEXAS INSTRUMENTS

2

AWR2944EVM · 76–81 GHz Automotive Radar

Architecture: single-chip FMCW radar SoC integrating the 76–81 GHz transceiver, ADC / processing resources and in-vehicle networking peripherals.

Clock evidence: AWR2944 publicly supports a **40 MHz crystal with internal oscillator**, a 40 MHz external oscillator, or an externally driven 40 MHz square / sine clock.

40 MHz Reference → Radar SoC → RF / ADC / DSP Domains

Selection insight: 76–81 GHz defines the radar RF operating band, while the external timing device is selected for the documented 40 MHz reference input.

RENESAS

3

R-Car V4H White Hawk · Multi-Sensor Fusion Compute

Architecture: R-Car V4H sensor-fusion platform supporting camera, radar and LiDAR data with 4 RGMII Ethernet, 2 CSI-2, 2 DSI, 2 PCIe Gen4 and 8 CAN channels.

Clock evidence: Renesas states that the platform replaces multiple crystal oscillators with a **programmable clock generator** to reduce BOM cost and mounting area.

Sensor Inputs → R-Car V4H → CSI / PCIe / Ethernet

Selection insight: high-integration fusion processors may use coordinated clock generation / distribution rather than one discrete oscillator per interface.

AMD

4

VEK280 / Versal AI Edge · High-Speed REFCLK Evidence

Architecture: adaptive SoC evaluation platform for sensor-fusion / AI development with processor, programmable logic and high-speed transceiver clock domains.

Clock evidence: VEK280 publishes **33.33 MHz LVCMOS PS clock**, **25 MHz LVCMOS Ethernet clock**, **100 MHz LVDS GT clock** and **156.25 MHz LVDS high-speed clocks**.

Processor / Ethernet → Adaptive SoC → 100 / 156.25 MHz GT

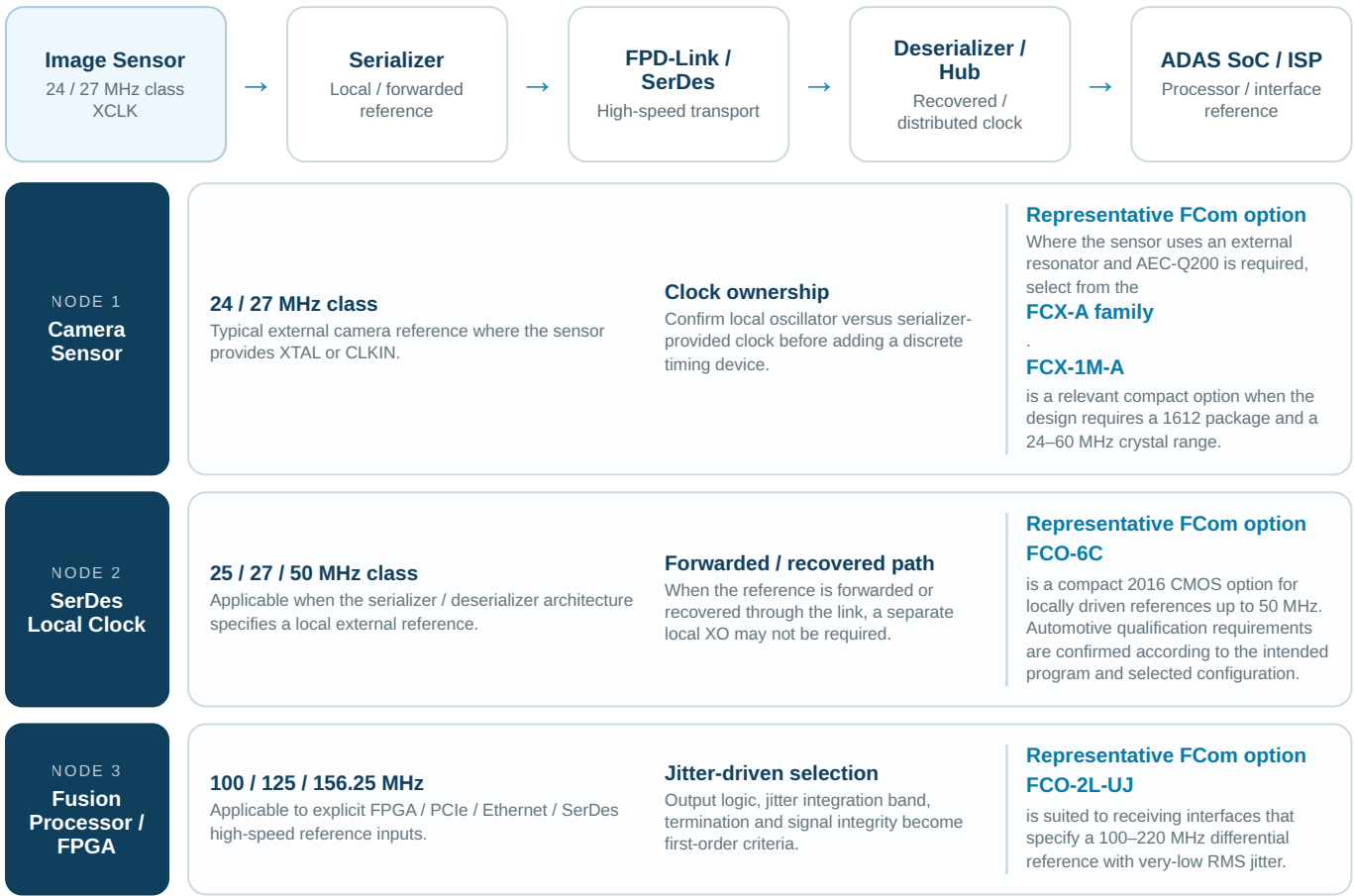
Selection insight: high-speed FPGA / SerDes nodes introduce explicit output-logic, jitter and termination requirements. VEK280 is used here as clock-tree evidence; the board itself is an evaluation platform.

Platform interpretation: these public examples are used to illustrate representative timing architectures. They do not indicate FCom adoption, qualification, compatibility or drop-in replacement. Final component selection is based on the exact target-device documentation, schematic and complete system requirements.

05

Multi-Camera / SerDes Timing Architecture

Representative placement of external timing from the camera module through the SerDes transport path to the ADAS processor.

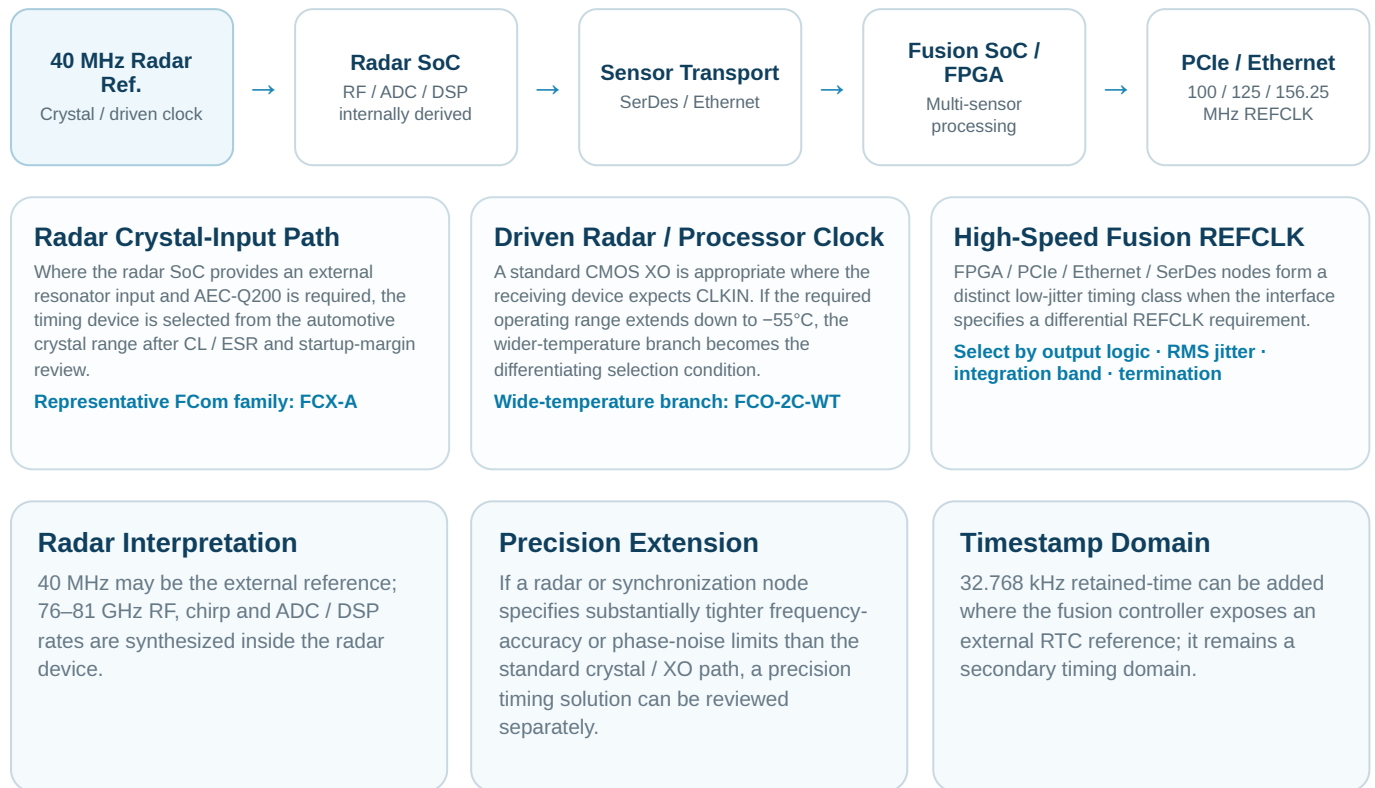


Design rule: timing-device placement follows the clock-distribution architecture. A dedicated local oscillator is used where the clock is generated locally; forwarded, recovered or centrally distributed clock paths may eliminate the need for an additional local device.

06

Radar + Multi-Sensor Fusion Timing Architecture

A representative radar, camera and high-speed fusion path showing where standard automotive references transition into low-jitter high-speed clock domains.



Architecture rule: sensor-fusion timing is evaluated by clock domain. Standard sensor and controller references, high-speed interface REFCLKs and retained-time references have different performance criteria and are selected independently within the overall ADAS architecture.

07

FCom Selection Guidance by Design Condition

The product families below correspond to the primary timing decisions in ADAS camera, radar, SerDes and sensor-fusion architectures. Exact ordering codes are confirmed after the receiving clock interface is defined.

Automotive Crystal Input

Camera / radar / controller XTAL input with AEC-Q200 requirement.

Driven CMOS Clock

Local sensor / SerDes / processor CLKIN, with temperature range as a selection branch.

Low-Jitter Differential REFCLK

FPGA / PCIe / Ethernet / high-speed SerDes.

Retained-Time

External 32.768 kHz RTC / event-timestamp reference.

Design Condition	FCom Selection	Why It Changes the Decision	Key Check Before RFQ
XTAL input + AEC-Q200	FCX-A family	Use the automotive crystal family for camera, radar or controller nodes that expose an external resonator input and require AEC-Q200. Exact package and series follow frequency, CL / ESR and startup-margin constraints.	Frequency · CL · ESR · startup margin · package
Driven CMOS CLKIN / local reference	FCO-6C FCO-2C-WT	FCO-6C covers the compact standard CMOS path up to 50 MHz, while FCO-2C-WT provides a wider-temperature option for designs requiring operation down to -55°C.	Frequency · VDD · ppm · temperature · OE / load
100–220 MHz + differential + explicit low jitter	FCO-2L-UJ	Applicable when FPGA / PCIe / Ethernet / SerDes interfaces specify a differential low-jitter reference. This is a distinct device class from standard camera or radar controller clocks.	LVDS / LVPECL / HCSL · jitter band · termination · VDD
External automotive 32.768 kHz	FCT-3M-A	Dedicated AEC-Q200 tuning-fork crystal for RTC / event-time / retained-time nodes that require an external 32.768 kHz resonator.	RTC topology · CL · ESR · standby requirement

Application-specific extensions: precision TCXO, VCXO, OCXO, programmable XO, spread-spectrum XO and RF/filter products can be evaluated when the system introduces specific accuracy, phase-noise, tuning, synchronization, EMI-management or filtering requirements. These device classes complement the core ADAS timing paths shown above where the corresponding function is required.

ENGINEERING SELECTION SUPPORT

Request an FCom ADAS Timing Recommendation

Provide the sensor / serializer / deserializer / radar / SoC / FPGA part number, clock node, local / forwarded / recovered topology, frequency, CL / ESR or supply / output, jitter / phase-noise targets, temperature, qualification and package constraints.

[Start Engineering Review →](#)

08

Engineering Validation & Minimum RFQ

ADAS timing selection requires clock-topology information in addition to frequency. Include the receiving IC and jitter / phase-noise requirements where applicable.

Camera / Sensor

- Image sensor / serializer / deserializer P/N
- XCLK / XTAL / CLKIN requirement
- Local, forwarded or recovered clock
- Frequency, CL / ESR or VDD / logic
- Allowable jitter / ppm and startup requirement

Radar

- Radar SoC / RF front-end P/N
- External reference frequency and input mode
- Crystal vs driven oscillator
- Phase-noise requirement if specified
- Local temperature and automotive qualification

FPGA / High-Speed

- FPGA / SoC / PHY / switch P/N
- 100 / 125 / 156.25 MHz or other REFCLK
- CMOS / LVDS / LVPECL / HCSL
- RMS jitter target and integration band
- Termination / load / supply / OE behavior

System Architecture

- Number of cameras / radar channels
- SerDes topology and clock distribution
- Fusion-processor architecture
- Retained-time requirement
- Prototype, qualification, EAU and SOP schedule

Minimum RFQ Information

Information Category	What to Provide
Application / Node	Camera module, radar sensor, SerDes hub, ADAS processor, FPGA / adaptive SoC, Ethernet / PCIe or retained-time node.
Target Device	Exact sensor / serializer / deserializer / radar SoC / processor / FPGA / PHY part number and the relevant clock pin or schematic section.
Clock Ownership	Is the clock locally generated, forwarded through SerDes, recovered from the link or distributed from another node?
Crystal	Frequency, package, CL, ESR, tolerance, temperature stability, drive level and AEC-Q200 requirement where applicable.
XO / High-Speed REFCLK	Frequency, VDD, CMOS / LVDS / LVPECL / HCSL, stability, temperature, RMS jitter / integration band, phase noise if required, termination and OE.
Project / Program	Prototype quantity, sample date, validation plan, annual volume, SOP timing, production site and environmental / qualification requirements.

Clock Topology First

Frequency alone does not determine the device class; the clock topology defines whether the appropriate solution is a crystal, CMOS XO, differential XO or a forwarded / recovered clock with no additional local timing device.

Jitter Where It Matters

Specify RMS jitter and integration band at explicit high-speed REFCLK nodes rather than applying the same requirement to every sensor clock.

Thermal & Qualification

Operating-temperature range and automotive qualification are separate selection attributes and are specified independently during component selection.

Frequency alone does not define the final component: a 25 MHz node can be a crystal-input sensor / PHY, a driven CMOS reference or part of a forwarded-clock SerDes architecture. The receiving IC documentation and system clock path determine the appropriate FCom solution.

09

Engineering FAQ & Application Review

Common ADAS clock-architecture questions, public reference sources and the information required for an FCom engineering review.

Does the image-sensor pixel clock equal the external crystal frequency?

No. Pixel clock and MIPI CSI-2 data rates are generated within the sensor / interface architecture. The external timing device is selected from the documented XCLK / XTAL / CLKIN requirement.

Does every serializer / deserializer require its own oscillator?

Not necessarily. Depending on the SerDes architecture, timing may be generated locally, forwarded over the link, recovered at the receiver or distributed from a common reference.

Is 76–81 GHz the radar crystal frequency?

No. It is the RF operating band. For example, TI AWR2944 publicly supports a 40 MHz crystal, external oscillator or driven 40 MHz reference as the external timing source.

When does RMS jitter become a primary selection parameter?

It becomes especially important at FPGA, PCIe, high-speed Ethernet and SerDes REFCLK inputs. Standard sensor / MCU clocks are usually driven first by frequency, stability and startup requirements.

Does every ADAS node require a differential oscillator?

Not necessarily. Camera, radar and processor reference nodes commonly use crystal or CMOS-clock architectures. Differential XO is selected where the high-speed receiver explicitly specifies LVDS / LVPECL / HCSL or equivalent differential REFCLK.

Does –40...+125°C automatically mean automotive qualified?

Not necessarily. Operating-temperature range and AEC qualification are separate attributes. Qualification is confirmed from the applicable FCom product specification and the documentation required for the automotive program.

Representative Public Technical References

1. **Texas Instruments:** TIDA-01413 — ADAS 8-channel camera + radar sensor-fusion hub with FPD-Link III clock synchronization.
2. **Texas Instruments:** AWR2944 — 76–81 GHz automotive radar SoC with documented 40 MHz crystal / oscillator / driven-clock options.
3. **Renesas:** R-Car V4H White Hawk — camera / radar / LiDAR sensor-fusion platform using a programmable clock generator.
4. **AMD:** VEK280 Clock Generation — public 25 MHz, 33.33 MHz, 100 MHz LVDS and 156.25 MHz LVDS clock-tree evidence.
5. **NDK:** Automotive ADAS / autonomous-driving block diagram — public node-to-frequency mapping for camera, radar, automotive computer and SerDes.

FCom product specification note: product information in this guide is presented at series or representative-configuration level. Exact ordering codes, qualification status, guaranteed limits and availability are confirmed against the applicable FCom product specification and quotation for the required frequency and electrical configuration.

ENGINEERING REVIEW

ADAS, Cameras & Sensor Fusion Timing Review

Provide the target sensor / SerDes / radar / SoC / FPGA, clock node, clock-ownership topology, frequency, CL / ESR or supply / output, jitter / phase-noise targets, operating temperature, qualification and project stage. FCom can review the requirement and recommend an appropriate timing series and configuration.

[Request Engineering Review →](#)
[FCom Solutions](#)

This guide provides representative application and product-selection guidance. Final component selection is confirmed against the latest target-device documentation and the applicable FCom product specification, followed by validation on the complete board and system.