

RADIO ACCESS & MOBILE NETWORK SYNCHRONIZATION

5G RAN, Small Cells & Mobile Transport

Frequency, phase and time synchronization for RU, DU, CU, small-cell and mobile-transport clock domains.

Frequency Traceability + Phase Alignment + Time Accuracy + Low Jitter

Radio Units

Distributed Units

Central Units

Small Cells

Fronthaul

Midhaul / Backhaul

Engineering Focus

Begin with the timing function: GNSS holdover, PTP / SyncE recovery, DPLL loop oscillator, radio device clock, Ethernet / SerDes clock or deterministic converter clock.

Engineering Consideration

The same nominal frequency can serve different clock domains. Stability, phase noise, pullability, RMS jitter, output interface, loop bandwidth and holdover behavior should be specified for each receiving node.

10 MHz

Common network reference and holdover interface.

122.88 MHz

Widely used RAN radio-clock family.

50 fs

Representative FCom 100-220 MHz UJ differential XO class.

1.5 GHz

FCom wide-frequency differential XO / VCXO range.

Application Scope & System Architecture

5G RAN, Small Cells & Mobile Transport includes 4G/5G radio access and its fronthaul, midhaul and backhaul equipment. A robust design transfers traceable frequency, phase and time from the network or GNSS source to radio, processing and transport clock domains without allowing one domain to compromise another.

Representative Equipment

RAN Radio & Edge

- Macro radio units and active antenna systems
- Indoor / outdoor small cells
- Repeaters and distributed antenna equipment
- Private-network radio nodes

Baseband & Compute

- Distributed units and central units
- O-RAN acceleration and baseband cards
- FPGA / SoC processing platforms
- JESD converter and radio-transceiver boards

Mobile Transport & Timing

- Fronthaul / midhaul / backhaul switches
- PTP grandmaster and boundary clocks
- SyncE network equipment
- GNSS-assisted timing gateways

Representative Synchronization Chain

GNSS / PTP / SyncE

Traceable time and frequency inputs



Reference Selection

Qualification · priority · protection



DPLL & Holdover

Servo · filtering · OCXO / TCXO / VCXO



System Clock Tree

1 PPS · ToD · 10 MHz · radio / SerDes clocks

Frequency

Transfer the long-term rate through SyncE, PTP or a physical reference while controlling wander.

Phase

Maintain inter-site and inter-radio alignment for TDD operation and coordinated radio functions.

Time

Preserve epoch and packet timestamp accuracy through 1 PPS, ToD and PTP paths.

Clock Quality

Keep phase noise, spurs and jitter within radio, converter and high-speed interface budgets.

FCom Solution Scope

FCom supports OCXO solutions for holdover and low close-in noise, TCXO solutions for compact wide-temperature references, VCXO solutions for controlled DPLL steering, and low-jitter differential XO solutions for radio, converter, FPGA and SerDes clock domains.

System-Level Performance

PTP accuracy, SyncE compliance, holdover and TDD phase alignment are determined at equipment level. Oscillator performance should therefore be evaluated together with the servo, clock IC, power, thermal and network architecture.

02

Select by System Node First

Define the clock function before choosing a frequency-control device. This separates holdover and loop-control requirements from radio and high-speed digital clock requirements.

System Node	Typical Function	Representative Frequency	Recommended Device Class	Selection Focus
Grandmaster / timing gateway	GNSS-disciplined source and autonomous holdover	10 MHz; 1 PPS / ToD are separate time interfaces	Low-noise OCXO; wide-temperature TCXO only where the holdover budget permits	Aging, warm-up, temperature stability, close-in phase noise, power
PTP / SyncE DPLL loop	Filter packet / physical timing and steer the local clock	10–52 MHz; architecture-specific 100 / 122.88 / 125 / 156.25 MHz	CMOS or differential VCXO matched to the clock-IC input and loop design	Pull range, control slope, loop bandwidth, phase-noise transfer
RU / small-cell radio clock	Transceiver DEVCLK, RF PLL reference or JESD clock-tree source	122.88 / 153.6 / 245.76 / 368.64 MHz	Ultra-low-jitter differential XO; wide-frequency XO only when a direct higher-frequency clock is required	RMS jitter bandwidth, output interface, deterministic SYSREF relationship
DU / CU / accelerator	FPGA, SoC, board SYSCLK and deterministic processing	100 / 122.88 / 125 / 156.25 MHz	100–220 MHz low-jitter differential XO	Interface, fanout topology, power noise, reset and phase alignment
Ethernet / SerDes transport	PHY, switch and optical-module reference	25 / 100 / 125 / 156.25 MHz	Low-jitter differential XO, or CMOS XO where the interface requires single-ended clocking	Standards mask, total jitter, load, EMI and link margin
Compact local reference	GNSS receiver, management SoC or small-cell controller	25 / 26 / 30.72 / 38.4 / 40 MHz	Compact TCXO or CMOS XO selected by stability, power and waveform	Package, power, temperature range, clipped-sine / CMOS interface

Holdover Node

Select from phase / time error accumulation, not nominal ppm alone. Aging learning and thermal profile can dominate the outage result.

Pullable Node

A VCXO is selected with the DPLL. APR, control voltage, gain, linearity and loop bandwidth must be reviewed together.

Fixed Low-Jitter Node

Specify the required interface and integration bandwidth. A jitter number is meaningful only with its measurement conditions.

Selection guidance: a published 122.88 MHz or 245.76 MHz clock—or a converter sample rate—should first be traced through the platform clock tree. The required clock may be synthesized from a lower-frequency VCXO or XO rather than supplied by a direct-frequency oscillator.

03

Frequency & Component Placement Matrix

These frequencies are recurring design anchors across RAN and mobile transport. Their actual role depends on the clock IC, radio profile, Ethernet interface and system partition.

Frequency / Signal	Common Placement	Clock Meaning	Recommended Device Class	Engineering Note
32.768 kHz	RTC / always-on domain	Low-power calendar and wake timing	Tuning-fork crystal or ultra-low-current kHz XO	Dedicated RTC function; separate from PTP, SyncE and radio phase references
10 MHz	Grandmaster, BITS / timing gateway, lab reference I/O	Traceable frequency and holdover anchor	Low-noise OCXO; TCXO only for a lower-power holdover class	Specify phase noise, aging, warm-up and outage objective
19.2 / 20 / 25 / 26 / 30.72 / 38.4 / 40 MHz	GNSS, modem / SoC, DPLL input or compact small-cell control	Local reference or synthesis input	TCXO, VCXO or CMOS XO selected by loop function	Confirm fixed versus pullable operation and input waveform
100 / 125 / 156.25 MHz	Ethernet, SerDes, switch, FPGA / SoC SYSCLK	Transport and deterministic digital clock	Ultra-low-jitter differential XO	Check output interface and standards-specific jitter mask
122.88 / 153.6 MHz	RAN clock tree, radio transceiver, baseband / JESD domain	Radio-rate family or device clock	Low-jitter differential XO; VCXO only for externally steered loops	SYSREF and multichip phase alignment are system functions
245.76 / 368.64 / 491.52 / 614.4 MHz	Radio DEVCLK, converter reference or synthesized clock tree	Higher radio / converter clock family	Wide-frequency differential XO; differential VCXO only when steering is required	Validate the final-frequency source against the jitter / phase-noise budget
983.04 / 1966.08 MSPS	FR2 / converter data path	Published sample-rate family	Derive the physical oscillator requirement from the clock tree	Confirm clock tree before XO selection
1 PPS / ToD	Epoch transfer and timestamp alignment	Time / phase markers, not free-running oscillator frequencies	Combine with a qualified frequency source and timing engine	Validate latency, cable delay, timestamping and failover

Frequency Path

SyncE and physical references transfer rate. The local oscillator and loop determine noise filtering and holdover.

Phase / Time Path

PTP, GNSS, 1 PPS and ToD provide alignment information. Packet delay variation and asymmetry remain system considerations.

Radio / Converter Path

JESD device clock and SYSREF must be generated and distributed deterministically; the oscillator is one stage in that chain.

04

Representative Platform & Architecture Matrix

Four public platforms illustrate how timing requirements differ between a network grandmaster, a baseband development system, a small-cell RF-sampling platform and an integrated radio transceiver.

MICROCHIP

TimeProvider 4100 Release 2.5

01

Telecom grandmaster / gateway clock with GNSS, IEEE 1588 PTP, SyncE, E1/T1, 1 PPS / ToD and 1 PPS / 10 MHz interfaces. Public oscillator options include OCXO, super OCXO and rubidium for different holdover objectives.

GNSS / PTP / SyncE → Servo + Holdover → PTP / 10 MHz / 1 PPS

Selection insight: the oscillator class follows the required outage duration, phase-error accumulation, warm-up and power budget; low-noise OCXO and wide-temperature TCXO address different holdover levels.

NXP

LA1224-RDB / LA12xx Development System

02

Public clocking includes 122.88 / 156.25 / 125 MHz SYSCLK options, 100 / 125 MHz clock generation, IEEE 1588, GPS, Ethernet and SerDes clocks. The platform also publishes FR1 sampling to 491.52 MSPS and FR2 modes at 983.04 / 1966.08 MSPS.

GPS / IEEE 1588 → Clock Generation → 122.88 / 125 / 156.25

Selection insight: 100 / 122.88 / 125 / 156.25 MHz nodes favor a low-jitter differential clock class. Published MSPS values describe the data path and should not be copied directly into an oscillator requirement.

TEXAS INSTRUMENTS

TSW4086 + AFE76xx Small-Cell Platform

03

The public dual-loop architecture locks PLL1 to an on-board 122.88 MHz VCXO. PLL2 produces few-gigahertz clocks and references; the LMK04610 generates a 368.64 MHz FREF plus FPGA reference and SYSREF.

122.88 MHz VCXO → Dual-Loop LMK04610 → 368.64 FREF + SYSREF

Selection insight: the pullable 122.88 MHz source must match the clock-IC input waveform, load, APR, control range and phase-noise mask. CMOS and differential interfaces are separate design paths.

ANALOG DEVICES

ADRV9029 Radio Transceiver

04

Four-transmit / four-receive radio transceiver with integrated RF and clock synthesis plus multichip phase synchronization. Public profiles use 153.6 or 245.76 MHz device clocks; the differential DEVCLK input accepts 15–1000 MHz and requires low phase noise.

Low-PN DEVCLK → Integrated Clock / RF PLLs → LO + Baseband Coherence

Selection insight: a focused ultra-low-jitter differential source may be evaluated inside its optimized frequency range; a wide-frequency differential source is considered when the device clock is required directly above that range.

Reference scope: these public platforms are included solely to illustrate published clock placement and frequency families. Final FCom component selection requires review of the target schematic and electrical requirements and does not represent original-platform qualification, pin-to-pin compatibility or endorsement.

05

GNSS / PTP / SyncE Timing & Holdover Architecture

A mobile-transport timing gateway qualifies multiple references, disciplines a local oscillator and maintains frequency / phase continuity through GNSS or packet-timing impairment.

LAYER 1 Timing Inputs	GNSS + 1 PPS / ToD Absolute time and phase source	PTP + SyncE Network time and frequency protection	Input Qualification Monitor validity, quality level, packet behavior, phase step and reference priority before steering.
LAYER 2 Servo & DPLL	Reference Selection Best source / hybrid source policy	Loop Filter Noise filtering and acquisition	Pullable Clock Class A VCXO is appropriate where the DPLL controls an external oscillator. APR, control range, gain and input waveform should be confirmed together.
LAYER 3 Holdover Source	OCXO Timebase Low-noise ppb-class holdover	TCXO Timebase Lower power / faster start	Primary FCom Node 10–40 MHz low-noise OCXO with stability to ± 5 ppb. Representative low-noise OCXO class · –120 / –145 / –157 / –162 dBc/Hz @10 / 100 / 1k / 10k
LAYER 4 Clock Generation	Physical Timing 10 MHz · E1/T1 · SyncE	Packet / Time PTP · NTP · 1 PPS · ToD	Alternative Stability Class Where the holdover error budget permits, a wide-temperature ± 50 ppb TCXO class can reduce size, power and warm-up time.
LAYER 5 Transport Outputs	Ethernet / SerDes 100 / 125 / 156.25 MHz	Fronthaul / Backhaul Boundary clock and SyncE distribution	Low-Jitter Digital Clock 100–220 MHz differential output for transport / FPGA clock domains. Representative 100–220 MHz low-jitter differential XO class · LVPECL / LVDS / HCSL · 50 fs

Application review: oscillator selection should follow definition of the system holdover target, phase-error allocation, oscillator learning model and thermal environment. Component stability is one element of the complete holdover specification.

06

Phase-Coherent Radio & Converter Clock Architecture

A radio node preserves network phase while generating low-noise device clocks and deterministic JESD timing for the transceiver, FPGA and converter domains.



Sample-rate interpretation: 491.52, 983.04 or 1966.08 MSPS may describe a converter or baseband data rate. The physical oscillator can be a lower-frequency reference multiplied by a PLL; the schematic clock tree therefore remains the basis for component selection.

07

FCom Selection Guidance

The following four decision gates translate defined clock-node requirements into practical FCom selection starting points. Final selection is completed against the target schematic and performance budget.

Decision 1 · Holdover Performance Class

FOC-5S-LN or **FVT-7S-WT**

OCXO direction: applications driven by close-in phase noise and ppb-class holdover. **TCXO direction:** applications prioritizing size, power and warm-up within a defined outage budget.

OCXO option: 10-40 MHz · ± 5 ppb · -162 dBc/Hz @10 kHz

TCXO option: 10-52 MHz · ± 50 ppb · -40 to $+105^\circ\text{C}$

Selection inputs: Outage duration · aging · phase error · thermal profile

Decision 2 · Externally Steered Loop

FVC-3X or **FVC-3L-PG**

A VCXO is appropriate where the DPLL / jitter cleaner steers an external source. The clock-IC input interface determines the applicable path.

CMOS option: 2-66 MHz · 2.8 / 3.3 V · ± 50 to ± 150 ppm

Differential option: 10-1500 MHz · LVPECL / LVDS · ± 50 to ± 150 ppm

Selection inputs: Input waveform · APR · loop bandwidth · PN mask

Decision 3 · 100-220 MHz Low-Jitter Clock

FCO-3L-UJ

Representative fixed-frequency starting point for 100 / 122.88 / 125 / 153.6 / 156.25 MHz radio, FPGA and transport clock nodes.

Package / Supply: 3225 6-SMD · 1.8 / 2.5 / 3.3 V

Output: LVPECL / LVDS / HCSL

Performance: ± 20 ppm · -40 to $+125^\circ\text{C}$ · 50 fs RMS jitter

Decision 4 · Direct Clock Above 220 MHz

FCO-3L-PG

Representative option where the schematic requires a fixed differential clock directly at 245.76 MHz or a higher radio / converter frequency.

Package / Supply: 3225 6-SMD · 2.5 / 3.3 V

Frequency / Output: 10-1500 MHz · LVPECL / LVDS

Performance: ± 25 ppm · -40 to $+105^\circ\text{C}$ · 0.6 ps RMS jitter

1 · Confirm Function

Holdover source, fixed low-jitter clock and pullable loop oscillator are different component functions.

2 · Confirm Clock Tree

Establish whether the final clock is supplied directly or synthesized by a DPLL / jitter cleaner.

3 · Apply the Budget

Use the specified phase-noise / jitter bandwidth, stability, temperature and interface limits to complete selection.

Configuration confirmation: FCom confirms the frequency-specific ordering code after reviewing exact frequency, voltage, output, stability, temperature, pullability, package and option requirements.

08

Engineering Validation & Minimum RFQ

Create one requirement set per clock node. A holdover oscillator, DPLL VCXO, radio DEVCLK and Ethernet reference should not be evaluated with the same acceptance criteria.

Node & Timing Profile

- RU, DU, CU, small cell, grandmaster or transport node
- PTP profile / clock role and SyncE requirement
- GNSS, PTP, SyncE, 1 PPS, ToD and external reference inputs
- Normal, protection and holdover operating modes

Frequency & Interface

- Exact oscillator frequency—not only the converter sample rate
- Sine, clipped sine, CMOS, LVDS, LVPECL or HCSL
- Supply, load, termination, logic level and enable behavior
- Fixed XO, VCXO / DPLL or disciplined OCXO / TCXO function

Stability & Holdover

- Initial tolerance and temperature stability
- Daily / monthly aging and powered-on learning interval
- Warm-up, retrace, reference-loss duration and phase-error budget
- Ambient, airflow, thermal gradient and enclosure behavior

Phase Noise & Jitter

- Phase-noise mask at exact offset frequencies
- Maximum RMS jitter and integration bandwidth
- Spurious limits and supply-noise sensitivity
- Clock IC additive jitter, PLL transfer and RF performance allocation

VCXO / Loop Parameters

- APR / pull range, control-voltage range and polarity
- Gain, linearity, center voltage and acquisition range
- DPLL bandwidth, damping and reference-switch behavior
- DAC resolution, noise and control-node filtering

Mechanical & Qualification

- Package, height, mounting and keep-out constraints
- Prototype quantity, sample date and EVT / DVT / PVT stage
- Annual volume, product life cycle and change control
- Required reports, screening and qualification expectations

Component Validation

Measure frequency offset, PN, jitter, spurs, pull response, warm-up, supply sensitivity and thermal behavior.

Clock-Tree Validation

Verify DPLL acquisition, reference switching, SYSREF relationship, deterministic reset and downstream fanout.

Network / Radio Validation

Measure holdover phase error, PTP / SyncE behavior, TDD alignment, JESD stability, EVM, ACLR and link margin.

Provide one requirement set per clock function. FCom Engineering can recommend the appropriate product series and ordering code. **Technical Review →**

09

Engineering FAQ & Application Review

Common RAN timing questions, representative public architecture references and the information required for FCom engineering review.

Why is 122.88 MHz common in RAN?

It belongs to widely used telecom sampling and clock families and appears in public baseband and small-cell clock trees. The system can use a direct 122.88 MHz source or synthesize it from another reference.

Is a published sample rate the oscillator frequency?

Not necessarily. Converter and baseband rates such as 491.52 or 983.04 MSPS can be generated from a lower-frequency reference through a PLL and divider tree.

OCXO or TCXO for holdover?

An OCXO should be considered when ppb stability, aging and phase-error accumulation drive the outage budget. A TCXO can reduce size, power and warm-up where the required holdover interval permits it.

Fixed XO or VCXO at the radio clock?

A fixed XO is appropriate when no external steering is required. A VCXO should be considered when the DPLL or jitter cleaner is designed to control the oscillator and its pull / phase-noise characteristics.

Does 1 PPS replace a frequency reference?

No. 1 PPS carries epoch / phase information but requires a continuous frequency source and timing engine for interpolation, noise filtering and holdover.

Can an FCom device be used as a direct replacement in a referenced platform?

The listed series provide functional selection starting points. Direct replacement requires confirmation of frequency, waveform, level, load, pullability, package, pinout, phase-noise / jitter mask and qualification requirements.

Public Architecture References

1. Microchip TimeProvider 4100 Series Release 2.5: official product brochure
2. NXP LA1224-RDB / Layerscape Access LA12xx Development System: official development platform page
3. Texas Instruments TSW4086 + AFE76xx small-cell reference design: official application report SLAA862A
4. Analog Devices ADRV9029 wideband RF transceiver: official data sheet

FCom product information: specifications are based on the current FCom product portfolio as of 20 August 2026. The applicable frequency-specific ordering code and final specifications are confirmed during application review.

Discuss Your RAN Timing Architecture

Send the equipment node, timing profile, exact clock frequency, output, supply, phase-noise / jitter target, stability and holdover requirement, temperature, package and prototype / annual volume.

[General Inquiry](#)
[Technical Support](#)